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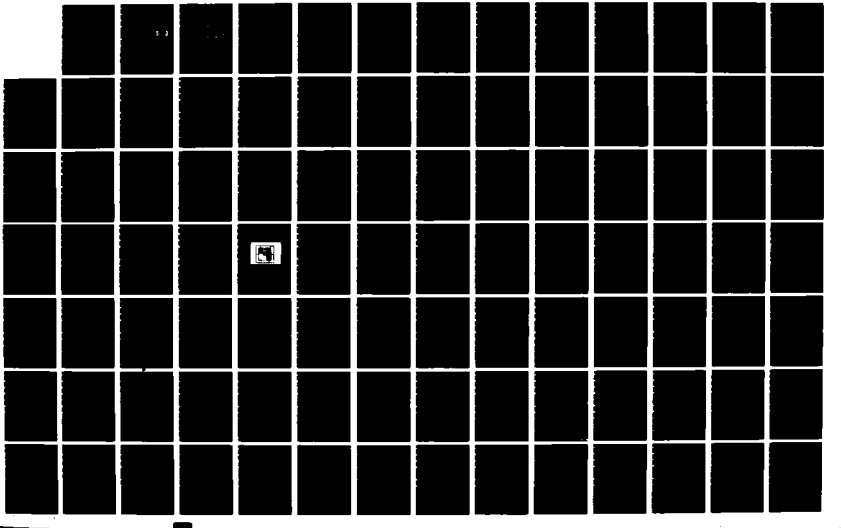

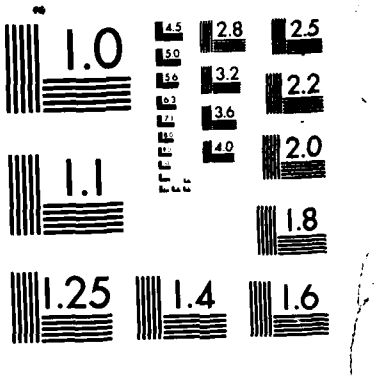

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A GaAs BASED DIGITAL SERIAL COMMUNICATIONS SYSTEM

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FINAL REPORT 25 MARCH 1986

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This thesis concerns the design and simulation of a one gigabit per second synchronous transmitter and receiver system. The circuitry is to be integrated on a 32-pin gallium arsenide semi-custom digital gate array. Digital logic components are built using enhancement and depletion mode n-channel metal-semiconductor field-effect transistors. The computer simulations indicate that, under a one micron gate process technology and using a 2V voltage

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supply, inverter propagation delays as small as 60 picoseconds can be achieved. Designs for both the transmitter and the receiver have been successfully simulated at the one gigahertz clock rate.

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A GaAs BASED DIGITAL SERIAL COMMUNICATIONS SYSTEM

BY

Ramon Z. del Rosario

THESIS

Submitted in Partial Fulfillment of the Requirements
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in Electrical Engineering
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A GaAs BASED DIGITAL SERIAL COMMUNICATIONS SYSTEM

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Santa Clara University, 1986

ABSTRACT

This thesis concerns the design and simulation of a one gigabit per second synchronous transmitter and receiver system. A very fast serial transmission rate can be achieved by integrating the circuit on a gallium arsenide (GaAs) semi-custom gate array. The 32-pin digital macro-cell gate array used requires only three masks for customization, making the turn-around time from design to fabrication relatively short. Digital logic components are built using enhancement and depletion mode n-channel metal-semiconductor field-effect transistors (MESFETs). The designs are implemented using state-of-the-art computer simulation packages, and the circuit layouts are drawn using a high-resolution graphics workstation. The simulation results indicate that, under a one micron gate process technology and using a 2V voltage supply, inverter propagation delays as small as 60 picoseconds can be achieved. Designs for both the transmitter and the receiver have been successfully simulated at the one gigahertz clock rate.

1. Introduction

The primary goal of this research project is to design and build a high-speed purely digital circuit on Gould Inc.'s macro-cell array (a GaAs semi-custom gate array chip). In order to ensure that the first test circuit for the macro-cell array will be successful, some restrictions have been placed on the application to be selected. One of these restrictions is that the circuit must be reasonably simple and feasible within the time frame of a master's thesis. Since the emphasis of the experiment is on speed, a very fast, digital serial data transmitter and receiver has been proposed. The requirement of the system to communicate data serially reduces the number of data lines to one and makes the system practical for a Local Area Network (LAN) application.

A simple way to make a serial communicator is to use shift registers to convert parallel data to serial data and vice-versa. The shift register size is determined by the characteristics of the macro-cell array. The gate array can accomodate as many as 500 logic gates, but to increase the yield, the actual number of gates used in this experiment is limited to about half the maximum. Mounted in a 32-pin package, the macro-cell array also limits the number of input and output lines the system can have. A system configuration that fits the requirements is a 16-bit shift register with sixteen parallel lines and one serial line. In this system, the shift register is sequenced by a 4-bit controller through 16 states. In order to test the gate array's capabilities near its limit, the target input clock rate is set at a fast one billion cycles per second (1 GHz).

It has been originally intended that both the transmitter and the receiver circuitry will be contained in one macro-cell array. With proper designing, the same shift register can be both serial in parallel out (SIPO)

and parallel in serial out (PISO). Similarly, one sequential controller can be made to control either a SIPO or a PISO register, depending on a select signal. For the time being, however, this approach is not used because the three-state devices required to allow sharing of the same I/O line are not yet feasible. Instead, the transmitter system and the receiver system are fabricated on separate macro-cell arrays. Also, because it is not possible to make an analog clock recovery circuit, a second transmission line is required to send the necessary reference clock signal.

Initial testing of the communications system design is accomplished through computer simulations. The task is made simpler with the development of an accurate GaAs MESFET model. The development is significant because the model can be used by ASPEC, a commercially available circuit simulation package already familiar to many circuit designers. Details of the simulations are given in Chapter 4. The flow chart on Figure 1-1 illustrates the design and testing process used.

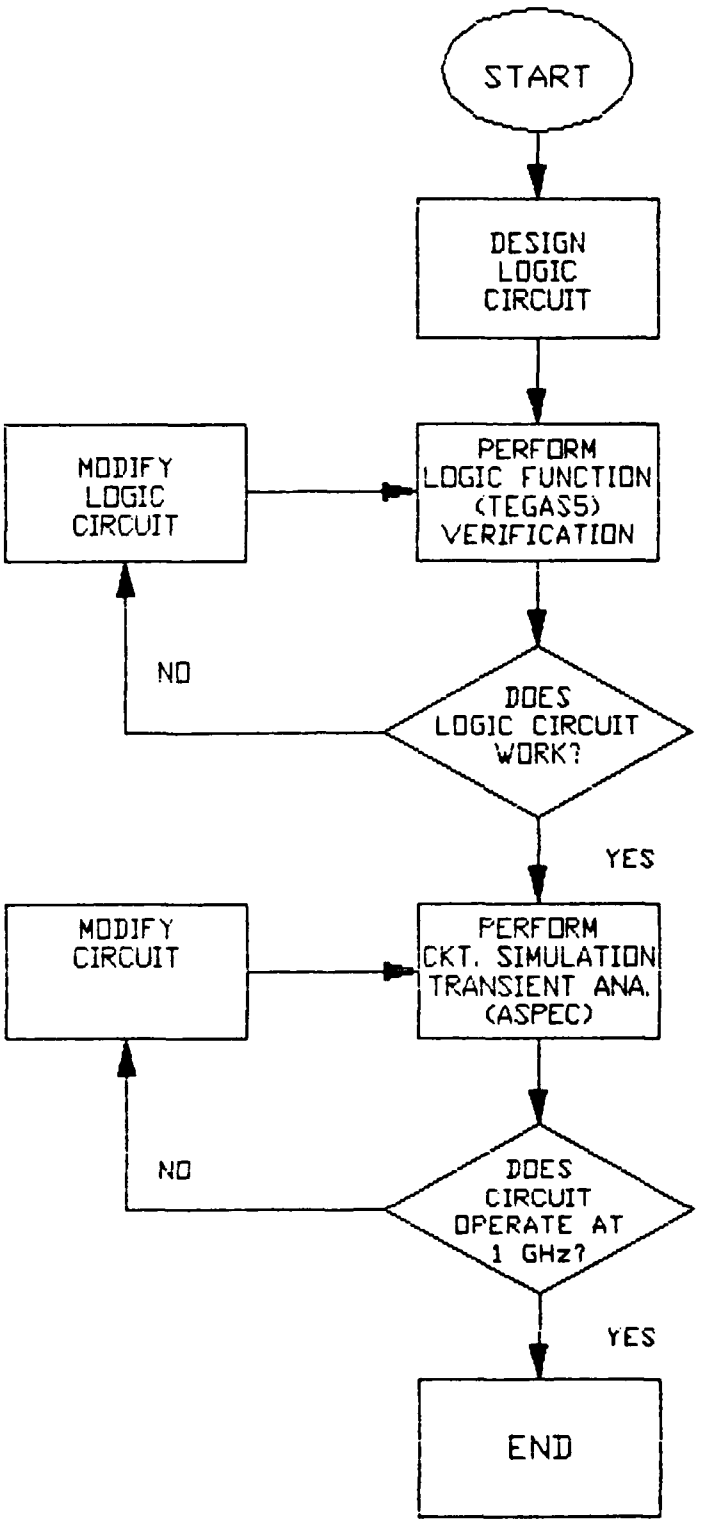


FIGURE 1-1. DESIGN/TEST PROCESS FLOW CHART

2. System Description and Operation

The configuration of the system chosen to be the first one integrated on the macro-cell array is a one gigahertz, synchronous transmitter and receiver with a 16-bit data size (see Figure 2-1). The transmitter will communicate with the receiver via two lines - one for the serial data and the other for the clock signal.

The transmitter system features a 16-bit parallel load shift register controlled by a 4-bit 16 state sequential controller. A common reset clears both the shift register and the controller asynchronously.

The sequential controller generates a LOAD signal once every 16 states, causing the binary data on the sixteen parallel input lines to be loaded into the shift register. At this point in the sequence, the first bit to be transmitted, bit 0, is present at the serial output pin. When the controller is clocked to the next state, LOAD is deasserted and SHIFT is asserted. The SHIFT signal remains until all sixteen bits have been transmitted, after which it is deasserted and LOAD is once again asserted to load the next data word.

The receiver circuit, like the transmitter, is basically a shift register and a controller. In this case, however, the 16-bit shift register is configured to convert serial data to parallel data. The register is continuously shifting and requires no control signals from the state machine. Because the data on the outputs of the shift register change at every shift, 16 S-R latches are used to save the data temporarily.

The purpose of the sequential controller is to generate the LATCH signal needed to store the 16 data bits into the array of latches. This signal, asserted once every 16 states, indicates that all 16 bits of the serial data have been received.

The task of the synchronizing, or SYNC, circuit is to ensure that the incoming data words are retrieved at the proper boundaries. The system reset, which clears the shift register and the state machine flip-flops, also resets the SYNC circuit and places it in the synchronizing mode. In this mode, the SYNC circuit hunts for a string of 16 consecutive ones, preceded and followed by at least one set of 16 zeroes, in the incoming serial data. After obtaining the word boundary information from the SYNC character, the SYNC circuit programs the controller to latch the data words accordingly. The SYNC circuit is automatically disabled after detecting the SYNC character to prevent resynchronizations due to the detection of a false SYNC character, for example, a string of 16 ones not contained within one word frame. At this point in the operation, hunting for a SYNC character ceases and all incoming bits are taken as transmitted data. Another system reset will re-enable the SYNC circuit.

For the purpose of circuit simplification, a hardware method of error detection and correction is not implemented.

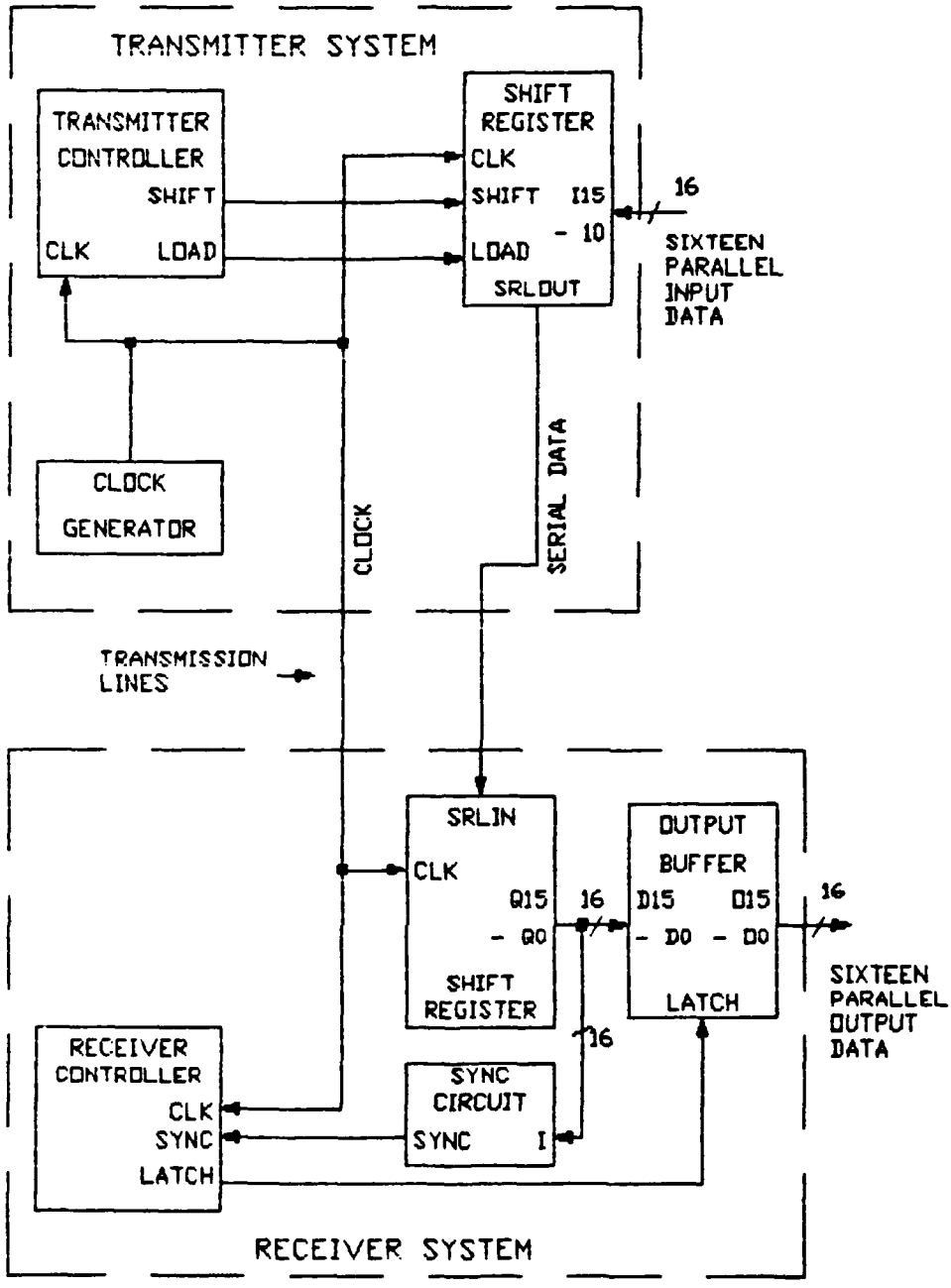


FIGURE 2-1. TRANSMITTER/RECEIVER SYSTEM BLOCK DIAGRAM

3. Circuit Description

THE SYNCHRONOUS TRANSMITTER SYSTEM

Figure 3-1 gives the logic circuit diagram of the synchronous transmitter system.

The Transmitter Register

The PISO shift register is made up of sixteen clocked D flip-flops with an input selecting circuit at each data input. The edge triggered flip-flop is chosen for its data lock-out feature. Depending on the control signals sent by the sequential controller, the input selecting circuit loads into the bit n flip-flop either the parallel input n or the Q output of the bit n+1 flip-flop. The flip-flops are numbered bit 15 (most significant bit) down to bit 0 (least significant bit) corresponding to parallel inputs I15 to I0. Data is shifted out of the Q output (SRLOUT) of the bit 0 flip-flop.

The Transmitter Controller

The transmitter controller (Figure 3-2) is a synchronous state machine built from four D flip-flops, labeled A through D. The system reset (RESET) clears the controller as well as the shift register flip-flops. All flip-flop SET inputs are disabled by connection to logic 0 (ground).

The input forming logic (IFL) of the machine is designed such that only one bit changes in each state transition. Because only NOR gates can be used, the IFL is implemented using a NOR-NOR instead of an AND-OR combination normally associated with a sum-of-product form. The NOR-NOR logic combination inverts the outputs of the flip-flops, but the effect presents no problems in this type of application.

The NOR based output forming logic (OFL) takes for its inputs Q-A, Q-B, Q-C, and Q-D. Thus, the output of the NOR gate rises when the state is at 0000 (state 0). Passed through an inverting super buffer (necessary for large fan-outs), this signal becomes the /LOAD signal for the PISO register. To derive the /SHIFT signal, the OFL signal is passed through an inverter before it enters another super buffer.

For handshaking, the /SHIFT signal can be connected to an output buffer and output pin to indicate that the transmitter is ready (TxRdy) to accept another data word.

The Clock Source

A ring oscillator consisting of eleven inverters generates the reference clock signal. The clock frequency can be varied by changing the voltage applied to the oscillator. For this reason, the oscillator has its own V_{cc} separate from the transmitter circuit V_{cc}. Applying the same voltage to both will set the frequency at approximately 1 GHz (assuming an inverter propagation delay of about 50 ps). A buffer cleans up and strengthens the clock signal for driving the clock inputs of the state machine flip-flops. A delayed version (due to additional buffering) of the state machine clock is used to clock the shift register. Later, it will be evident from the timing analysis that the delaying is necessary for the proper loading of the shift register.

THE SYNCHRONOUS RECEIVER SYSTEM

Figure 3-3 gives the logic circuit diagram of the synchronous receiver system.

The Receiver Register

The SIPO register of the receiver is similarly constructed as the PISO register of the transmitter except without the input selecting logic. The Q output of the bit n+1 D flip-flop connects directly to the D input of the bit n flip-flop. The input of the bit 15 flip-flop is the serial input (SRLIN) of the register. Thus, the way data bits are shifted into the receiver is compatible with the way they are shifted out of the transmitter.

The Output Buffer

A Set-Reset (S-R) latch flip-flop is connected to the Q and /Q outputs of each D flip-flop in the shift register. The sixteen S-R flip-flops form the output holding register, which serves to hold the 16-bit data received. The function is necessary, since the external device reading data from the receiver will most likely be too slow to read the data straight from the shift register. At a 1 GHz clock rate the data at the outputs of the shift register changes every 1 ns. On the other hand, the data in the output holding register change only every 16 ns.

The SYNC Circuit

The synchronizing (SYNC) circuit (Figure 3-5) can be divided into two sections - the SYNC character detecting section and the SYNC disabling section. The SYNC detector consists of four 4-input NOR gates which have, for inputs, the sixteen /Q outputs (/Q15 to /Q0) of the shift register. The outputs of these NOR gates are inverted and are then connected to four of the five inputs of the 5-input buffered NOR gate. When the shift register is filled with ones, its /Q outputs go to zero. Depending on the condition of the fifth input pin of the buffered NOR, a SYNC signal is then generated.

The buffered NOR gate takes its fifth input from the output (SYNCOFF) of the SYNC disabler. When the circuit is in the SYNC character hunt mode, this output (the Q output of a D flip-flop) is low and the buffered NOR is enabled. When a SYNC character is detected, however, the resulting SYNC signal and the subsequent falling edge of the system clock cause SYNCOFF to go high, which, in turn, disables the buffered NOR and deasserts the SYNC signal. The disabling signal remains high and no other SYNC characters are detected until the system has been reset.

The Receiver Controller

The design of the receiver state machine is nearly identical to that of the transmitter's (Figure 3-4). The difference lies in the inclusion of an additional input to the IFL. This input is for the SYNC signal generated by the SYNC circuit. The signal, when asserted, forces the state machine to go to state 0001 (state 1) at the next state transition.

The OFL is configured such that an output is generated when the state machine is in state 0010 (labeled as state 15). The latch signal generator takes the OFL signal and, because of propagation delays of the logic circuit, generates /LATCH within state 0000 (state 0). The contents of the shift register during state 0000 are thus loaded into the output holding register.

For handshaking, the /LATCH signal can be used to indicate that data is ready (RxRdy) at the parallel outputs of the receiver.

For both the transmitter and the receiver, output signals (O15 - O0, RxRdy for the receiver; TxRdy for the transmitter) are passed through noninverting output buffers before connection to output pins. Input signals (RESET, SRLIN for the receiver; RESET, I15 - I0 for the transmitter) are passed through 50 ohm pull-down resistors and super buffers before they are

connected to the main circuitry. In the special case of the SRLOUT and the CLOCK outputs from the transmitter, the signals are passed through line drivers capable of driving either a coaxial cable system or a fiber optic transmission system.

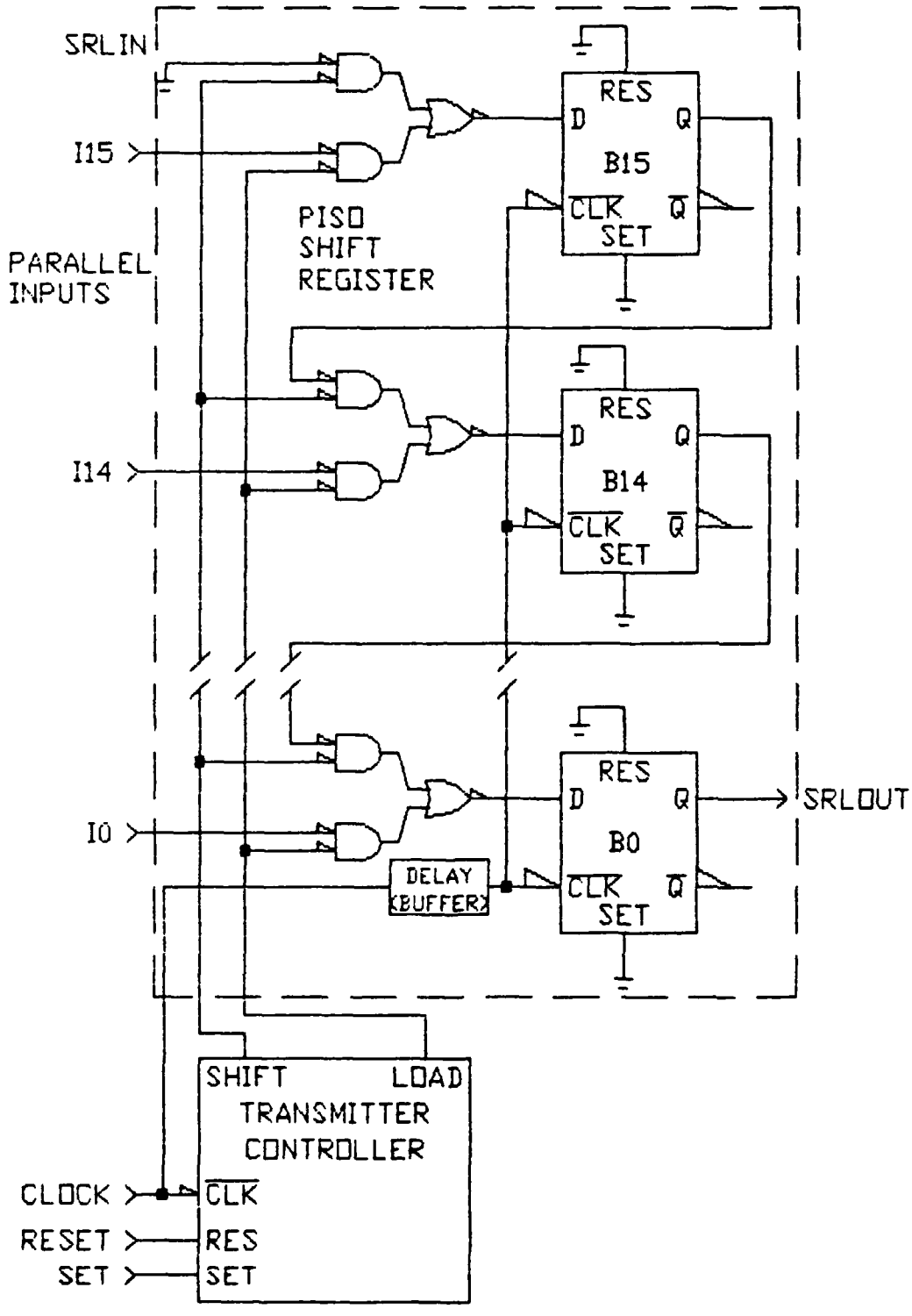


FIGURE 3-1. TRANSMITTER - LOGIC DIAGRAM

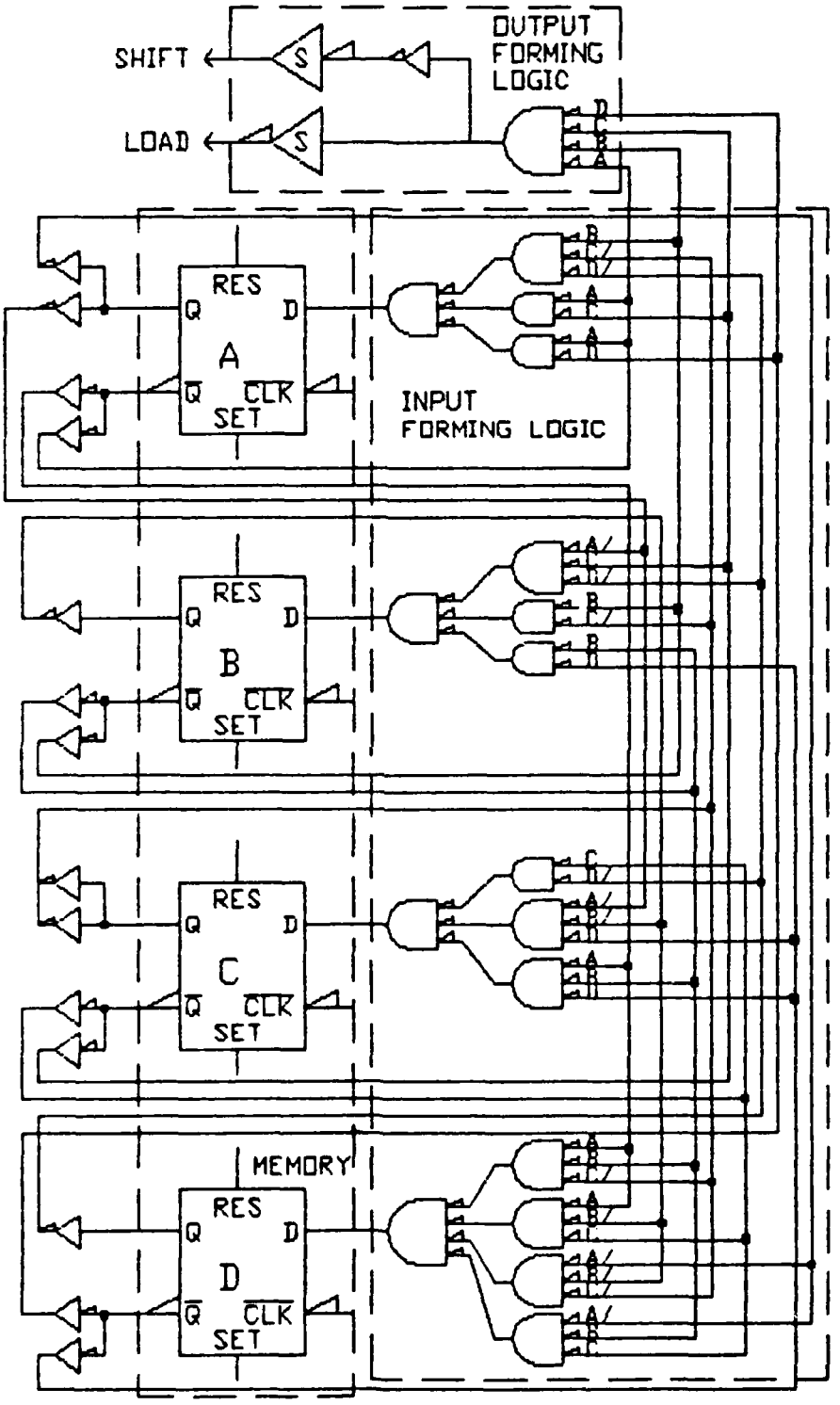


FIGURE 3-2. TRANSMITTER CONTROLLER

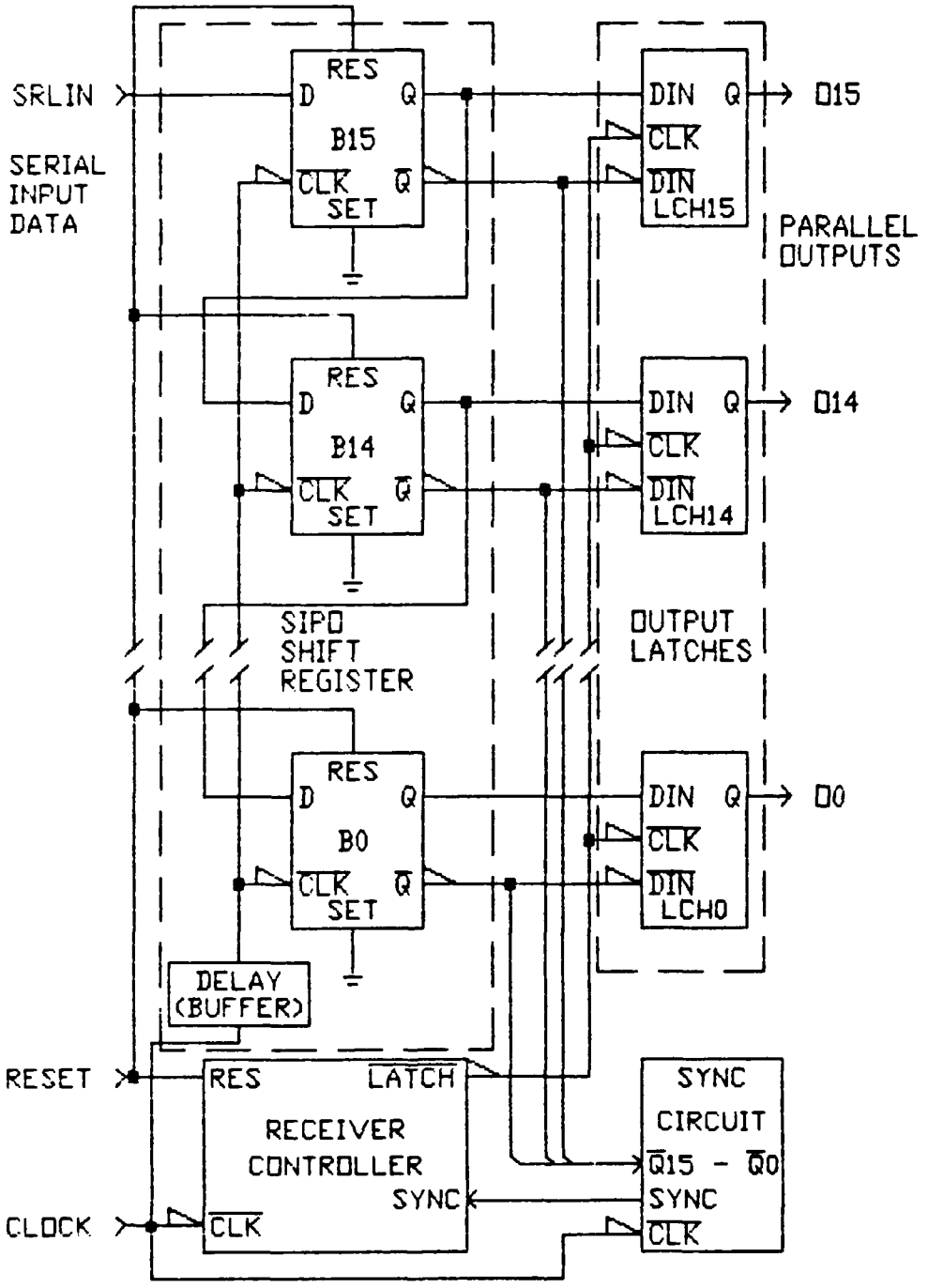


FIGURE 3-3. RECEIVER - LOGIC DIAGRAM

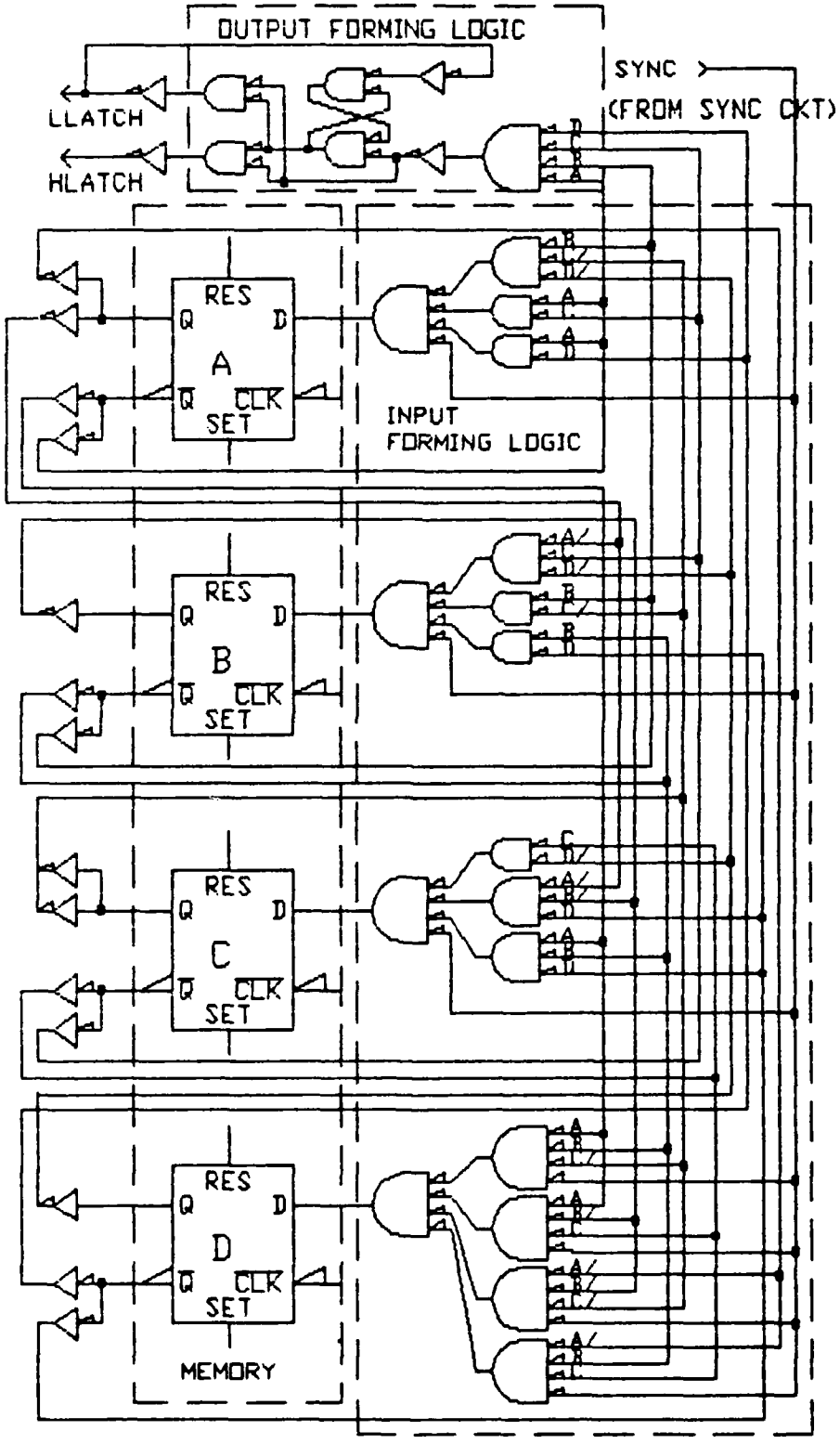


FIGURE 3-4. RECEIVER CONTROLLER

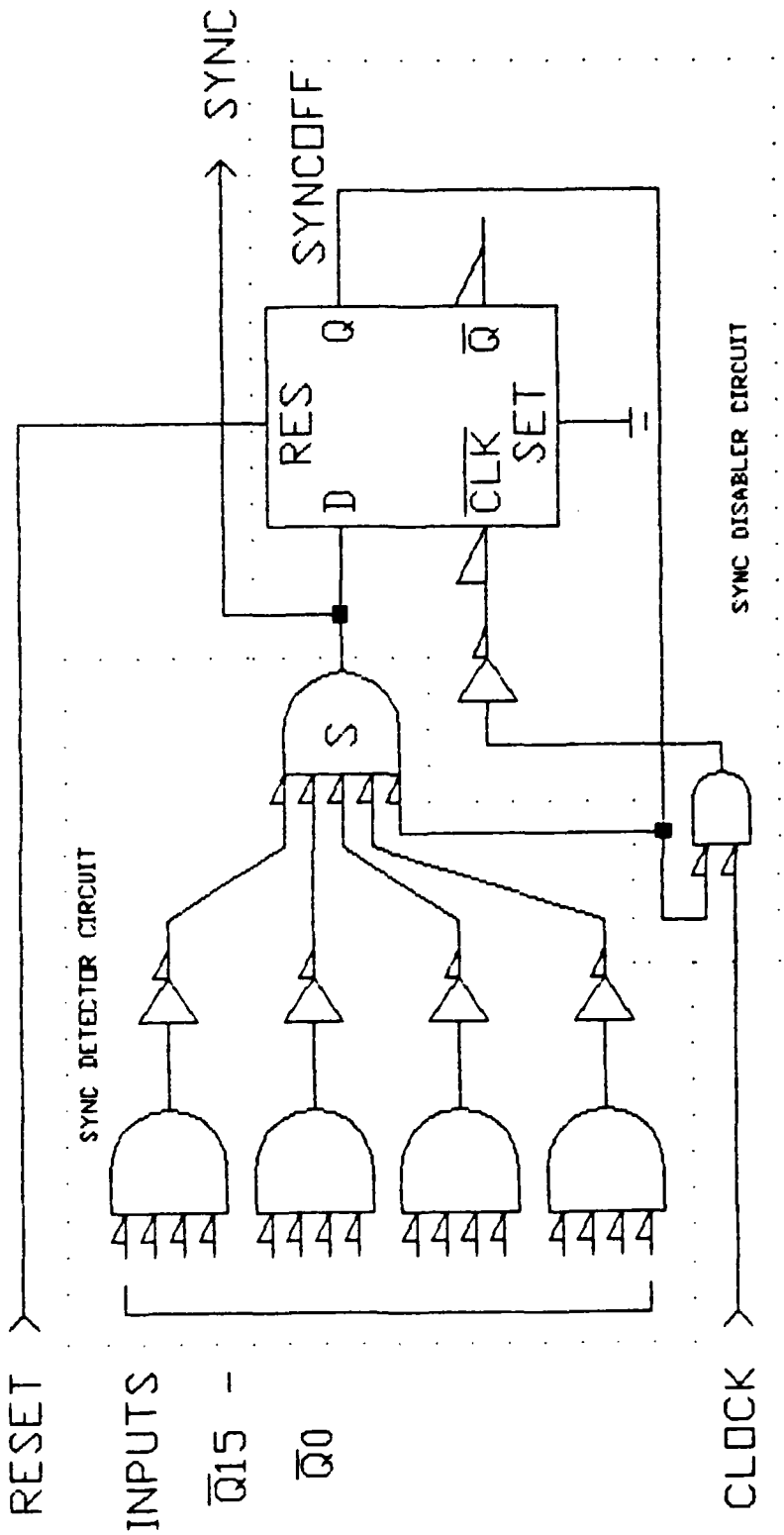


FIGURE 3-5, SYNC CIRCUIT

(S INDICATES BUFFERED LOGIC GATE)

4. Computer Simulations

After the functions of the system have been specified, the system can be designed. The designing process is made easier through the use of computer simulation packages.

A simulation package called TEGAS5 has been used to test initial configurations of the system [1]. This digital logic simulation and test generation system is available through Control Data Corporation's CYBERNET Services network. The software is practical during the early stage of the design process since it is relatively simple and inexpensive. The simplest mode allows logic function verification and rudimentary timing analysis. For a more sophisticated analysis of the circuit, however, a circuit simulation package is required.

Circuit simulation allows integrated circuit designers to make a model of the circuit at the transistor level and perform, among other things, transient analysis. The simulation package used is ASPEC (Advanced Simulation Program for Electronic Circuits) version 8H, also available through Control Data [2].

MESFET DEVICE TRANSFER FUNCTION ANALYSES

At present, no MESFET model exists in the ASPEC library of devices. Fortunately, the n-channel MOSFET model that does exist is sophisticated enough to permit customization so that it can be used to emulate a GaAs n-channel MESFET. Credit for the work belongs to Mr. Al Matthews, designer of the macro-cell array and former manager of Gould - Microwave Products Division's GaAs Digital IC Engineering.

The MOSFET model comes with numerous variable parameters, but it is only necessary to set a few, the majority of which are process-related, in order to

achieve the desired results. The process-related parameters and their values are:

VT	Threshold Voltage	= -0.5 V for depletion mode
		= 0.15 V for enhancement mode
UB	Low Field (Bulk) Mobility	= 3500 $cm^2/(V*sec)$
TOX	Gate Oxide Thickness	= 300 angstroms
DNB	Bulk Doping Concentration	= $1 * 10^{17}$ cm^{-3}
VMX	Scattering Limited Velocity	= $2 * 10^7$ cm/sec

The remaining parameter values are BULK = 0 (substrate is ground) and CLM (channel length modulation) = 1. The gate length is set to 0.6 micron.

All process parameters, with the exception of UB and TOX, come from actual device measurements. The values for UB and TOX have been obtained by trying several values for each in the MOSFET model and observing the I-V curve generated each time the model is simulated. The procedure is continued until the simulation I-V curve comes close to the I-V curve obtained from experiments. The CLM parameter is set to 1 to give the I-V curve a more realistic positive slope in the saturation region (the default value 0 gives a slope of 0 in this region). Although the physical gate length of each device is 1 micron, the value used in the model is the effective gate length of 0.6 micron obtained experimentally.

Results from the device simulations can be found in the Appendix starting from page 41. For all simulation outputs, voltage is given in volts, current in milliamperes, time in seconds, and temperature in Celsius (set at 25 degrees C).

To complete the model, a diode should be placed between the gate and the source of the FET to simulate the diode-like effects of the junction between the gate metal and the n-channel, particularly the area between the gate and the source. The direction of the diode current flow is from gate to source. The diode model parameter values are:

IS	Reverse Bias Saturation Current	$= 1 * 10^{-14}$ amps
CJA	Zero-Bias Junction Capacitance	$= 1 * 10^{-14}$ farads
RS	Series Resistance	= 100 ohms

These diode parameters are part of the small-signal equivalent circuit of the MESFET, and need to be included in the model only if transient analysis is performed.

COMPLEX CIRCUITS AND TRANSIENT ANALYSES

The E-D Inverter

Once the model of a GaAs n-channel MESFET is obtained, a logic gate and even a digital logic circuit can be simulated. The simplest logic gate to model first is the enhancement input to depletion load (E-D) inverter. Figure 4-1 shows the schematic of the E-D inverter model. In the case of this as well as in other similar applications, the diode between the gate and the source may be omitted if the gate is shorted to the source. The omission saves some computer time, especially when large, complex logic circuits are involved.

The output file printout from the E-D inverter transfer function analysis is listed on page 46, followed by the inverter transient analyses. To obtain the transfer function, the input voltage is swept from 0 to 0.8 V. The

voltage supply is set at 1 V. The results of the transient analysis, performed on three 10 micron input to 3 micron output (10/3) inverters in series to simulate loadings, give an inverter propagation delay of about 60 ps (which closely matches measurements made in the laboratory and thus should give confidence that the quasi-MESFET model is adequate). Also included are transient analyses of inverters with E/D combinations of 10/4.5 and 10/6. The results show smaller propagation delays and sharper rises, but also smaller logic swings. The latter combinations are not normally used, except in places where delays and fan-outs are critical.

The Line Driver

The next circuit simulated is the coaxial cable line driver (Figure 4-2). The transient analysis output is on page 52. For this and the rest of the simulations in this paper, the voltage supply is set at 2 V. The line driver consists of a super buffer (the first four stages) followed by a fat, 500 micron wide E-mode inverter with a 1 k ohm resistor load. The super buffer has the effect of boosting and sharpening the input signal, and is very useful when dealing with large fan-outs or very large input devices. The line driver is noninverting, with a total propagation delay of about 320 ps. The linear resistor load pulls up the output to 2 V.

The Output Buffer

A similar circuit to the line driver is the output buffer (Figure 4-3; simulation output on page 52). The final stage, however, is a 200/60 inverter. The output buffer is used for boosting output signals before they are connected to the output pins. The total propagation delay of the output buffer is approximately 220 ps.

The three remaining simulations involve the use of logic NOR gates (schematic in Figure 7-1 (b)). In order to facilitate and simplify the simulation of these large digital logic circuits, macro definitions are employed. Macros allow one to define a group of basic elements as a single functionl block that can be used like a circuit component. Once defined, it can be called as often as possible within the circuit description through the use of macro expansions. Use of macros, however, does not save memory; it merely makes the simulation input file easier to write and read.

The D Flip-Flop

The first of the logic circuit simulations is the D flip-flop simulation (logic diagram in Figure 4-4; simulation output on page 54). The D flip-flop is set up as a toggle flip-flop in order to illustrate the propagation delay of the device (measured from CLOCK input node 10 to output node 80). The propagation delay is 275 ps. One half of this value gives the typical propagation delay of a NOR gate (fan-out = 3, fan-in = 3). The value obtained, when compared with the delay of an inverter with a fan-out of one, shows that a fan-out of N increases the propagation delay by a factor of approximately N [6].

The Transmitter and Receiver System

The last two simulations address the main objective of this study - to build a 1 GHz GaAs digital transmitter/receiver system. Figures 4-5 and 4-6 give the logic circuit diagrams of the transmitter anad the receiver, respectively. The circuits simulated are reduced but accurate versions of the systems described earlier. Redundancies exist, particularly in the shift register sections, which can be eliminated without sacrificing the integrity

of the simulations. For both cases, the sequential controller remains intact. In simulating fan-out loadings, gates proportional to the omitted loads have been added to compensate for the reduction. This approach cuts down on processor time as well as costs.

The transmitter system

The input file for the transmitter system transient analysis begins on page 55. Before arriving at this final form, several versions have been written and rewritten in order to produce the desired output. The same is true for the receiver system, as well. This process comes after a preliminary design is obtained from TEGAS simulations. ASPEC lets the designer simulate and look at the propagation delays at any point in the circuit. The designer can thus determine if the circuit is going to work (or not) and make the appropriate changes before the circuit is fabricated. Buffers can be placed at paths with critical fan-out problems (at the expense of delaying the signals) and additional propagation delays can be added to fix skew problems.

The outputs generated by the transmitter input file starts from page 59. The first transient plot contains information on controller signals /SHIFT (VSHFT) and /LOAD (VLOAD) and its effects on the contents of the (reduced 2-bit) shift register. The shift register clock (VCLKD) is a delayed version of the state machine clock (VCLK) - the goal here is to move the falling edge of the shift register clock to within the boundary of the negative pulse LOAD signal so that the load function will work. With shift register input I1 set to a logic one and input I0 set to zero, the output of bit 1 (VO1) goes to one while bit 0 (VSRO) remains at zero after the load operation. The subsequent shift operation (clock falling edge while /SHIFT is asserted) causes the

output of bit 1 to go to zero as bit 0 goes to one. Another shift leaves both outputs at zero.

The second plot displays the state of the sequential state machine and the status of the shift register input selecting logic, and is useful in circuit debugging. To reduce the simulation time length, the state machine has been set to 0010 (state 15, effectively skipping over states 0 to 14). At the next clock falling edge, the controller will advance to state 0000. While at this state, the OFL is asserted and the control signals are generated (see the first plot).

The receiver system

The last ASPEC simulation is the receiver system transient analysis (input file listing begins on page 61). For this simulation, the OFL is modified such that it is asserted when the controller is at 0100 (state 3) instead of at 0010 (state 15). The simulation time span thus is reduced by removing states 4 to 15 from the simulation.

Three output plots are generated (printouts begin on page 66). The first displays the status of the state machine (VQA, VQB, VQC, VQD; state outputs VSO and VNSO), and the latch signal generator (outputs VBQ, VST, VLCH) in relation to the system clock (VCLK). The second printout displays the outputs of the latch registers VO3 - VO0 in relation to the two versions of the clock (VCLK for the state machine; VNCLK for the shift register), the /LATCH signal, and the serial input VIN. The last printout gives the status of the SYNC circuit (SYNC detecting section - VLNBL, VLNOT, VPROG; SYNC disabling section - VSCLK, VNSCLK, VDOFFQ) in relation to the system clock and the contents of the shift register (VR3 - VR0).

The rise in the SYNC signal VPROG indicates that the shift register is filled with ones. The signal causes the state machine to go to state 0001 at the next VCLK falling edge and the receiver is now synchronized. The VPROG signal also causes the rise of the SYNC disabling signal VDOFFQ at the next VCLK falling edge. This signal, in turn, causes the VPROG to fall. When the state machine reaches state 0100, the /LATCH signal VLCH is again generated and the data in the shift register are loaded into the output holding register.

An examination of printout #2 shows how serial data is received. Ignoring the first falling edge of VNCLK (since RESET is still asserted), the subsequent four falling edges shifts in four ones and the SYNC character is formed. The 4-bit character that follows is 1010 (received LSB first). By the time the character is fully formed in the shift register, the controller asserts the /LATCH signal and saves the character in the latch register.

In actual implementation and testing, the transmitter system and the receiver system will be interfaced by two equally sized coaxial cables - one for serial data and the other for the main clock signal. Since the propagation delay through the cable varies with its length, the skew between serial data and clock can be adjusted by using at least one coaxial cable with a minutely variable length.

FULL SYSTEM LOGIC SIMULATIONS - TEGAS5

Finally, the circuit designs obtained through ASPEC are translated back into TEGAS input files (page 69). With TEGAS, it is possible to simulate the complete system over a longer time interval without incurring excessive costs. Delay elements have been added to simulate the delays observed through ASPEC. The outputs begin on page 74.

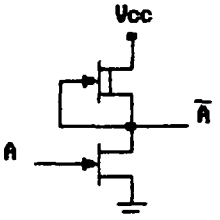


FIGURE 4-1. INVERTER

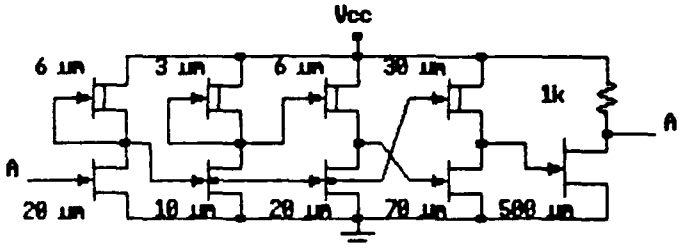


FIGURE 4-2. COAXIAL CABLE LINE DRIVER

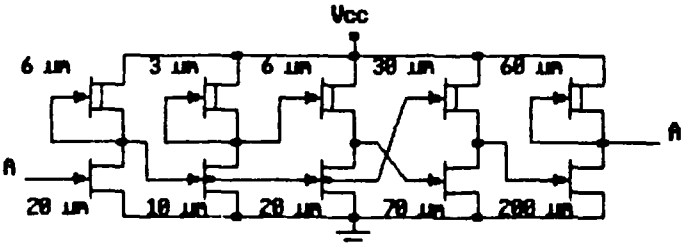


FIGURE 4-3. OUTPUT BUFFER

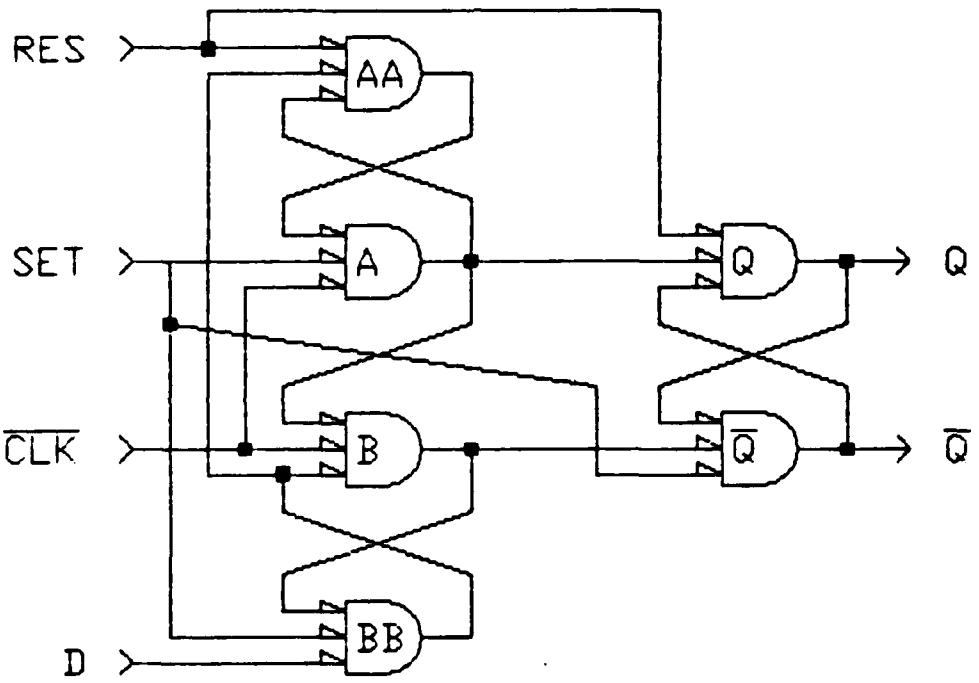


FIGURE 4-4. D FLIP-FLOP LOGIC DIAGRAM

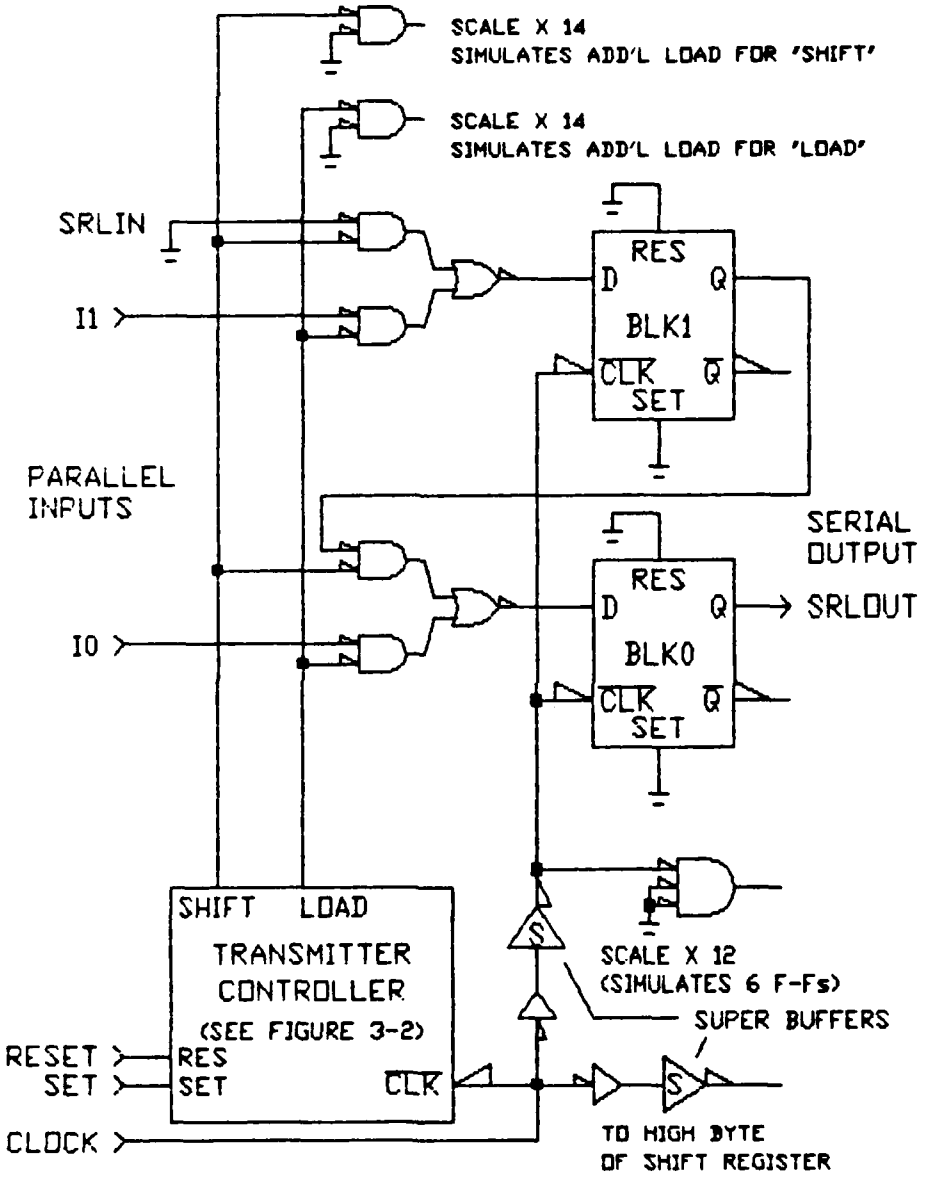


FIGURE 4-5. TRANSMITTER SYSTEM - REDUCED MODEL

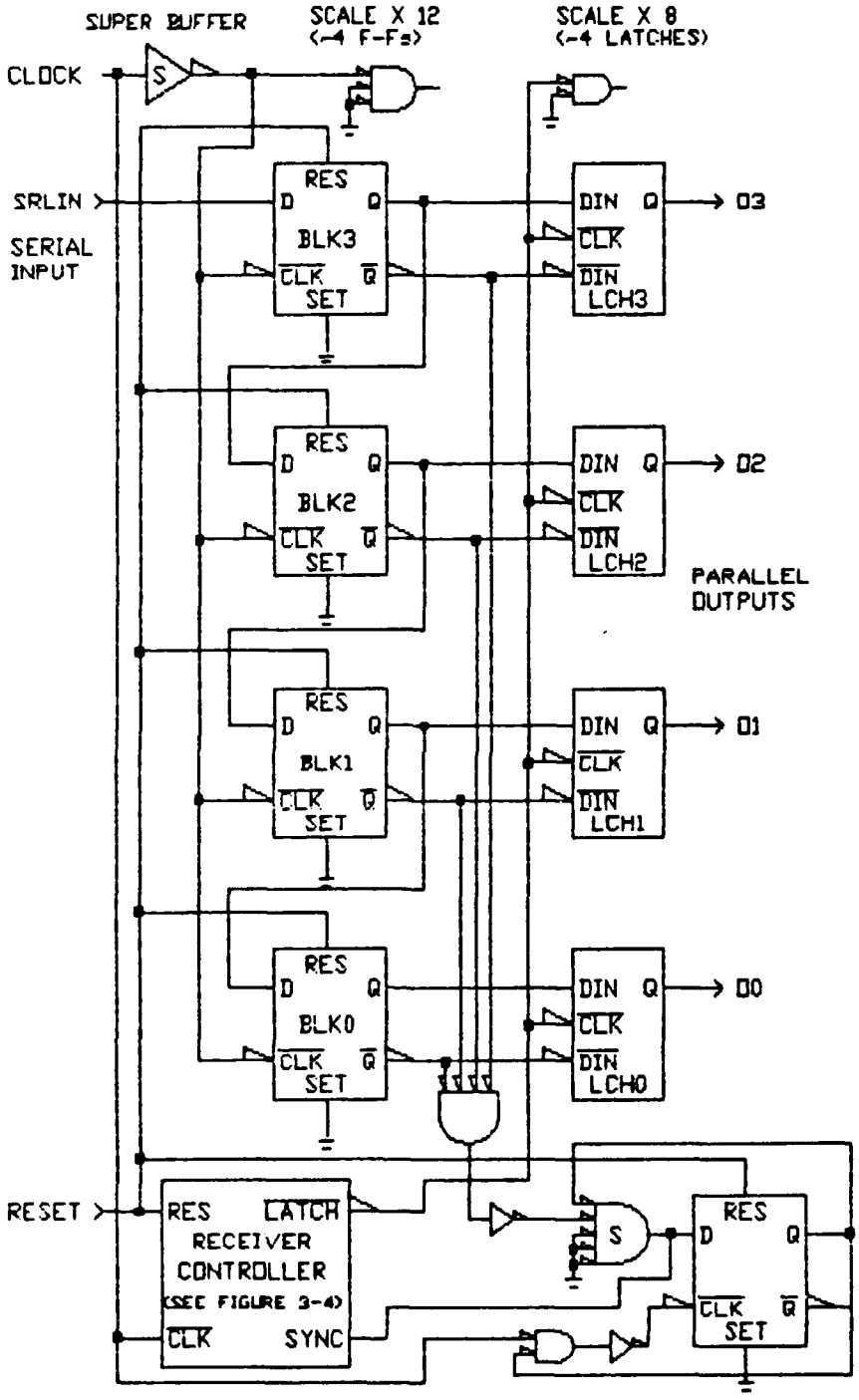


FIGURE 4-6. RECEIVER SYSTEM - REDUCED MODEL

5. The Macro-cell Array

Currently under development, the Macro-cell Array is Gould, Inc.'s first venture into the GaAs gate array field. A similar product named the Quick-Chip is already in production at Tektronix, Inc. [4]. Unlike the Quick-Chip, however, the macro-cell array contains digital devices exclusively - analog functions are not supported. In addition, the macro-cell array can accomodate larger circuits.

The development of the macro-cell array serves several purposes, the most important of which is to test Gould's new GaAs processing technology. Once fabricated, macro-cell arrays will provide system designers a way to integrate in one package fairly large and complex digital circuits with gigahertz clock rates and low power consumption. Customizing the macro-cell array for a particular application requires the user to design and fabricate only three masks.

The inner section of the macro-cell array consists of ninety-six macro-cells divided evenly into two rectangular groups separated by an approximately 140 micron wide horizontal gap. Arranged within each rectangular group are four rows of nine macro-cells. This inner array occupies a 1325 micron by 1370 micron area.

Surrounding the inner array and forming the square perimeter of the whole macro-cell array are thirty-two input/output (I/O) cells - eight I/O cells on each side and spaced 225 microns apart. In each space between I/O cells is an I/O pad. There is a total of thirty-two I/O pads for connection to the outside world. There is ample space between the inner array of macro-cells and the outer array of I/O cells and between the two halves of the inner array for hefty power bus lines. The whole macro-cell array fits into a 1900 micron wide square area.

Inside each 125 micron by 150 micron macro-cell are two columns of input devices, with ten devices in each column. Each device is an enhancement mode n-channel MESFET with a 10 micron width and a 1 micron gate length. Between the two columns is a column of eight nonlinear load devices. Each of these depletion mode n-channel MESFETs has a 1 micron gate length and a width selectable to 3, 4.5, or 6 microns, depending on how the source and drain are wired.

The input/output cell permits the construction of signal buffers and drivers. Occupying a 100 micron by 100 micron area, an I/O cell contains two 6 micron and two 30 micron depletion devices. Also contained are four 20 micron enhancement (or E) MESFETs, two sets of 35 micron E-MESFETS each with two parallel gates, and two sets of 35 micron E-MESFETS each with seven parallel gates. By connecting in series the parallel gates in a set, larger devices can be made available. For instance, connecting all seven gates on the 35 micron MESFET will yield a 245 micron enhancement device. However, no more than one device can be fabricated in each set. All devices in the I/O cell, like the devices in the macro-cell, use the one micron technology. Each I/O cell also contains two, 5 micron by 20 micron resistors, available for pull-ups and pull-downs.

6. Circuit Implementation on the Gate Array

Integrating the transmitter and the receiver using macro-cell arrays is not a difficult task. Because a macro-cell array is preprocessed up to the gate metal layer of the transistors, integrating a custom circuit design on it takes less time and only requires three levels of metallization (hence three masks) for transistor interconnects. The three mask layers are, from bottommost to topmost, metal 1, via, and metal 2.

Metal 1 is used to interconnect the devices on the surface of the (uncustomized) macro-cell array. For the most part, these lines run horizontally (parallel to the 140 micron gap described earlier).

Raised above metal 1 by a dielectric layer, the metal 2 layer serves to bridge over metal 1 layer obstacles such as active transistors and other metal 1 lines. These lines generally run vertically. Metal 2 is preferred over metal 1 for power wirings because of its greater conductivity.

The middle mask layer, the via layer, allows metal 1 connections to be brought up to the metal 2 level. This mask causes holes to be etched through the dielectric layer to metal 1 lines underneath so that metal 1 and metal 2 will connect when the metal 2 layer is deposited.

There are a few simple layout rules to be followed in designing circuits for the macro-cell array. Wire width must be 1 micron minimum for metal 1 and 2 microns minimum for metal 2, although it is a good practice to make the wires wider, especially when they run long or carry strong signals. Wirings on both metal levels are to be done at a minimum 2 micron pitch. Finally, the minimum crossover for contact between gate metal and metal 1 and between metal 1 and via is set at 1 micron.

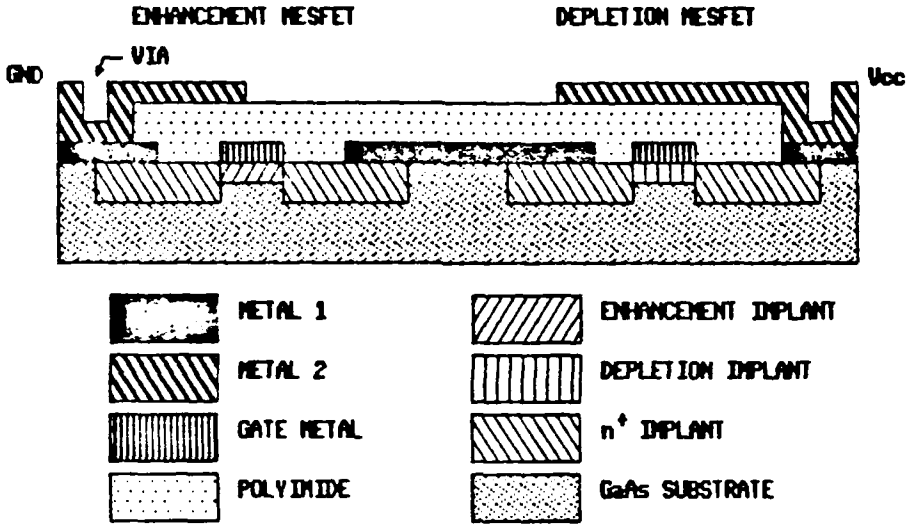
7. Circuit Layout

Availability of 10 micron E-mode inputs and 3, 4.5, and 6 micron D-mode loads makes possible the implementation of direct-coupled FET logic (DCFL) gates. Construction of a logic gate is simple (see Figure 7-1). Although NAND gates are possible, they are not used because they prove to be unreliable when fabricated using this particular GaAs process [6]. The designer is thus restricted to NORs and inverters when constructing a digital circuit.

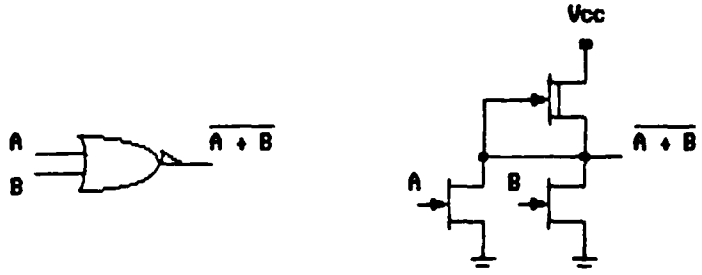
Figure 7-2 illustrates the implementation of a falling edge triggered D flip-flop using one macro-cell (the wide vertical lines are metal 2 wires). The flip-flop features an asynchronous SET and RESET and is the basis of most of the functional blocks in the transmitter and receiver system. Figure 7-3 shows how two S-R latches fit inside one macro-cell.

A screen from the CAD graphics system used to design the circuit layout is shown in Figure 7-4. The wide red rings surrounding the inner array of cells are the power wirings discussed earlier. The blue lines represent metal 1 lines.

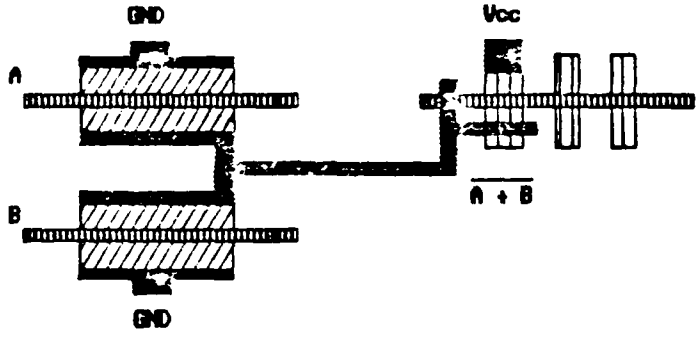
The photograph shows the transmitter circuit at 90% completion, sufficient enough to illustrate the layout of the major sections. The clusters at the top left and at the bottom right of the inner array constitute the PISO shift register. The two columns of macro-cells on each of the far edges are the shift register flip-flops and the inner column on each side makes up the input selectors. The eight macro-cells located at the upper right are occupied by the state machine. The ring oscillator is the cluster at the bottom left of the inner array.



a) IC CROSS SECTION



b) SCHEMATIC



c) IC LAYOUT

FIGURE 7-1. NOR GATE

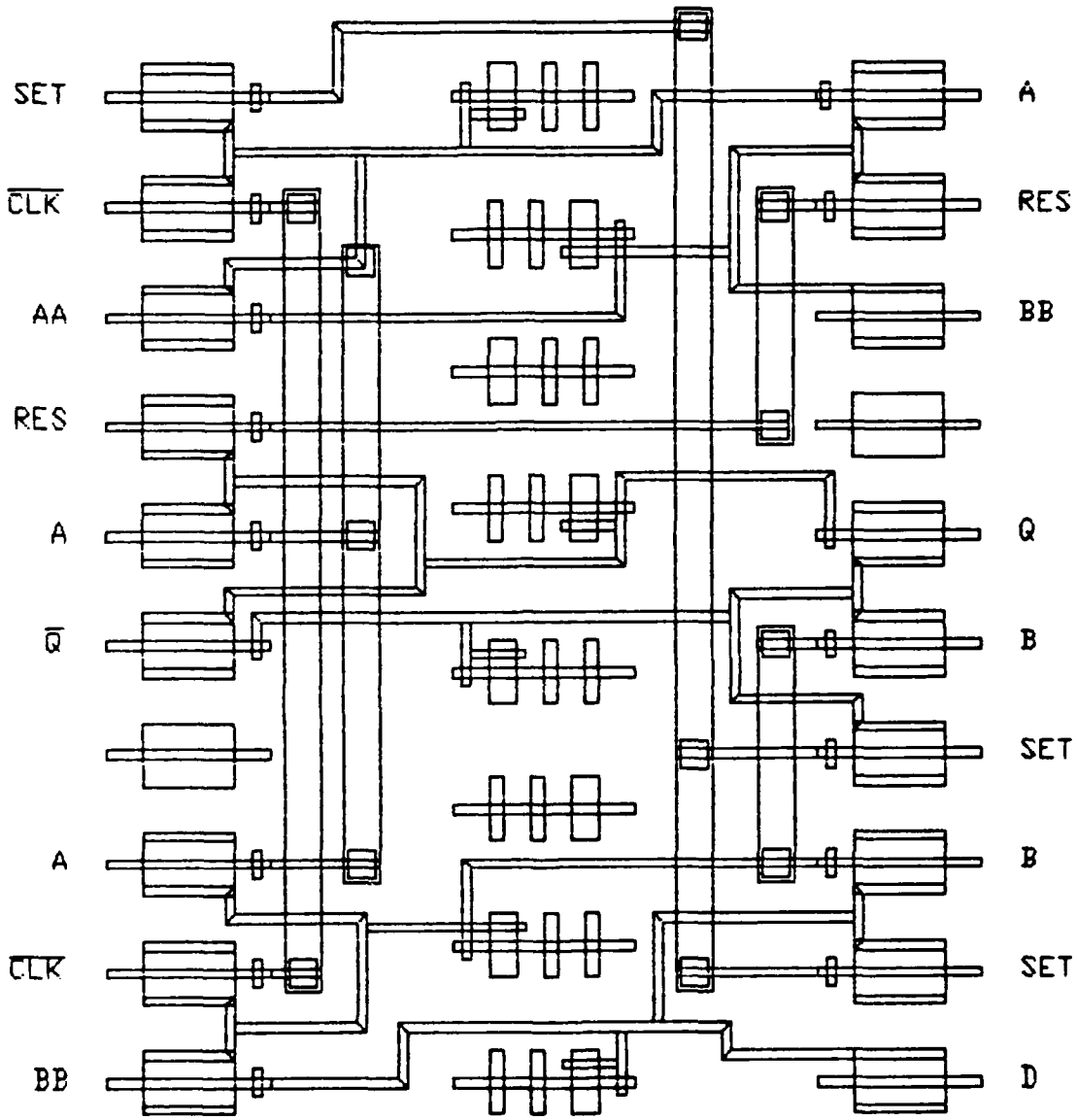


FIGURE 7-2. D FLIP-FLOP

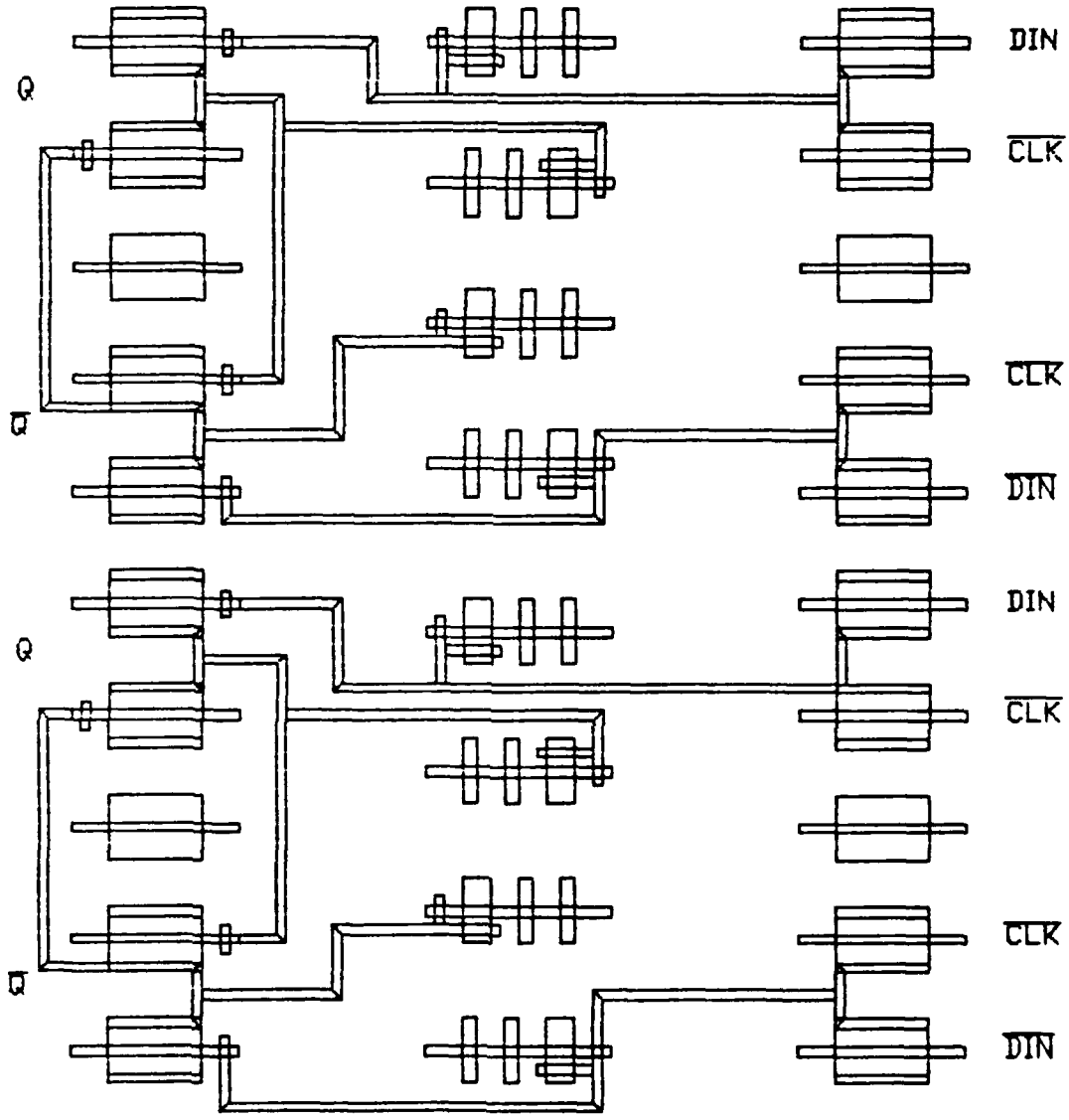


FIGURE 7-3. TWO D LATCH FLIP-FLOPS

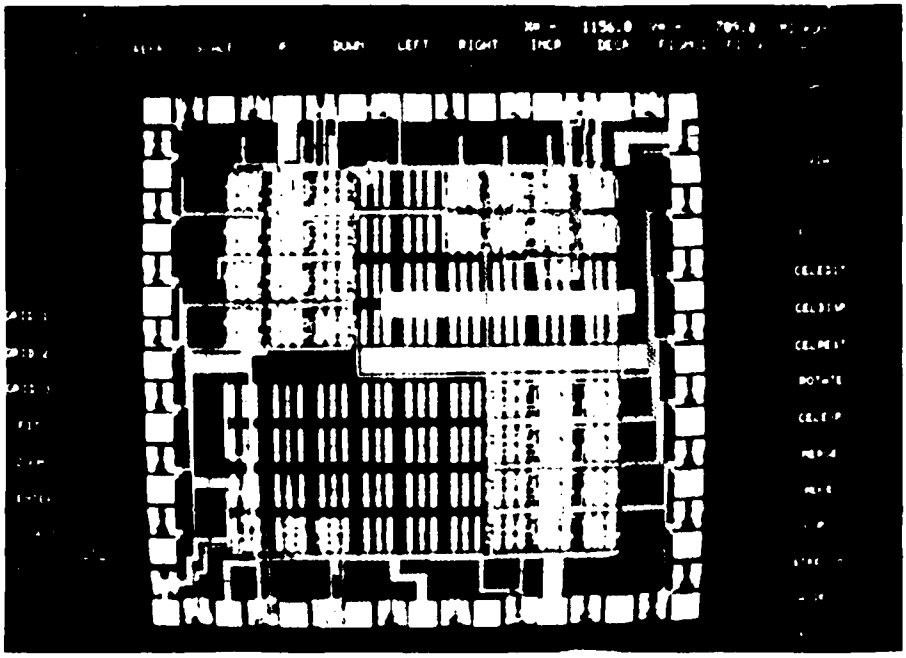


FIGURE 7-4. PHOTOGRAPH OF CAD SCREEN - MACRO-CELL ARRAY

8. Conclusion

The circuit design for a 1 GHz transmitter and receiver system, to be implemented on Gould, Inc.'s GaAs macro-cell array, has been completed. Used with either a coaxial cable system or the more state-of-the-art fiber optics system, the communications system can function effectively in a local area network, in anticipation of future demand for extremely fast data transmitting capability.

Through computer simulations, which necessitated the creation of a GaAs MESFET model, the operations of the the transmitter and the receiver have been tested and demonstrated. Typical propagation delays obtained from the simulations are in line with those obtained from actual measurements. For a simple inverter, a delay of about 60 ps has been obtained. More complicated circuits, particularly NOR gates and amplifiers, produce even larger delays. Problems with the circuit designs encountered in the course of the simulation are identical to problems that may be encountered in actual device testing. For instance, the simulations show that, as the circuits become larger and more complex, the degradation of signal levels due to larger fan-outs become more and more of an issue (a common problem in MESFET-based circuits). Remedies such as amplifiers sacrifice speed for signal integrity. Because the use of NAND gates is not allowed (because of process limitations), the logic circuit design is less efficient and is, therefore, slower. It is still possible to design a communications system to run at 1 GHz (as has already been demonstrated), but the system will require a slight re-design (mainly skew adjustments) in order to run it at faster clock rates, even if the difference is not that great.

Work on the masks required for the customization of the gate arrays is near completion, but the macro-cell array is not yet ready for fabrication.

For further work, the circuit designs can be implemented on the macro-cell array and tested. It may even be a good idea to reduce the data size to 8 bits so that both the transmitter circuit and the receiver circuit can be built on the same chip.

REFERENCES

[1] Control Data Corporation, TEGAS5 Simulation and Test Generation System Reference Manual, 1981.

[2] Control Data Corporation, Advanced Simulation Program for Electronic Circuits (ASPEC) User's Manual.

[3] M. Helix, S. Hanka, P. Vold, and S. Jamison: "A Low Power Gigabit IC Fabrication Technology," IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest 1984, pp. 163-166, 1984.

[4] L. Pengue, G. McCormack, E. Strid, D. Smith, and T. Bowman: "The Quick-Chip: A Depletion Mode Digital/Analog Array," IEEE Gallium Arsenide Integrated Circuit Symposium Technical Digest 1984, pp. 27-30, 1984.

[5] R. Eden, A. Livingston, and B. Welch: "Integrated Circuits: The Case for Gallium Arsenide," IEEE Spectrum, vol. 20, No 12, pp. 30-37, Dec. 1983.

[6] S. Long, B. Welch, R. Zucca, P. Asbeck, C-P. Lee, C. Kirkpatrick, F. Lee, G. Kaelin, and R. Eden: "High Speed GaAs Integrated Circuits," Proceedings of the IEEE, vol. 70, No 1, pp. 38-45, Jan. 1982.

[7] A. Rode, and J. Roper: "Gallium Arsenide Digital IC Processing - A Manufacturing Perspective," Solid State Technology, vol. 28, No 2, pp. 209-315, Feb. 1985.

APPENDIX

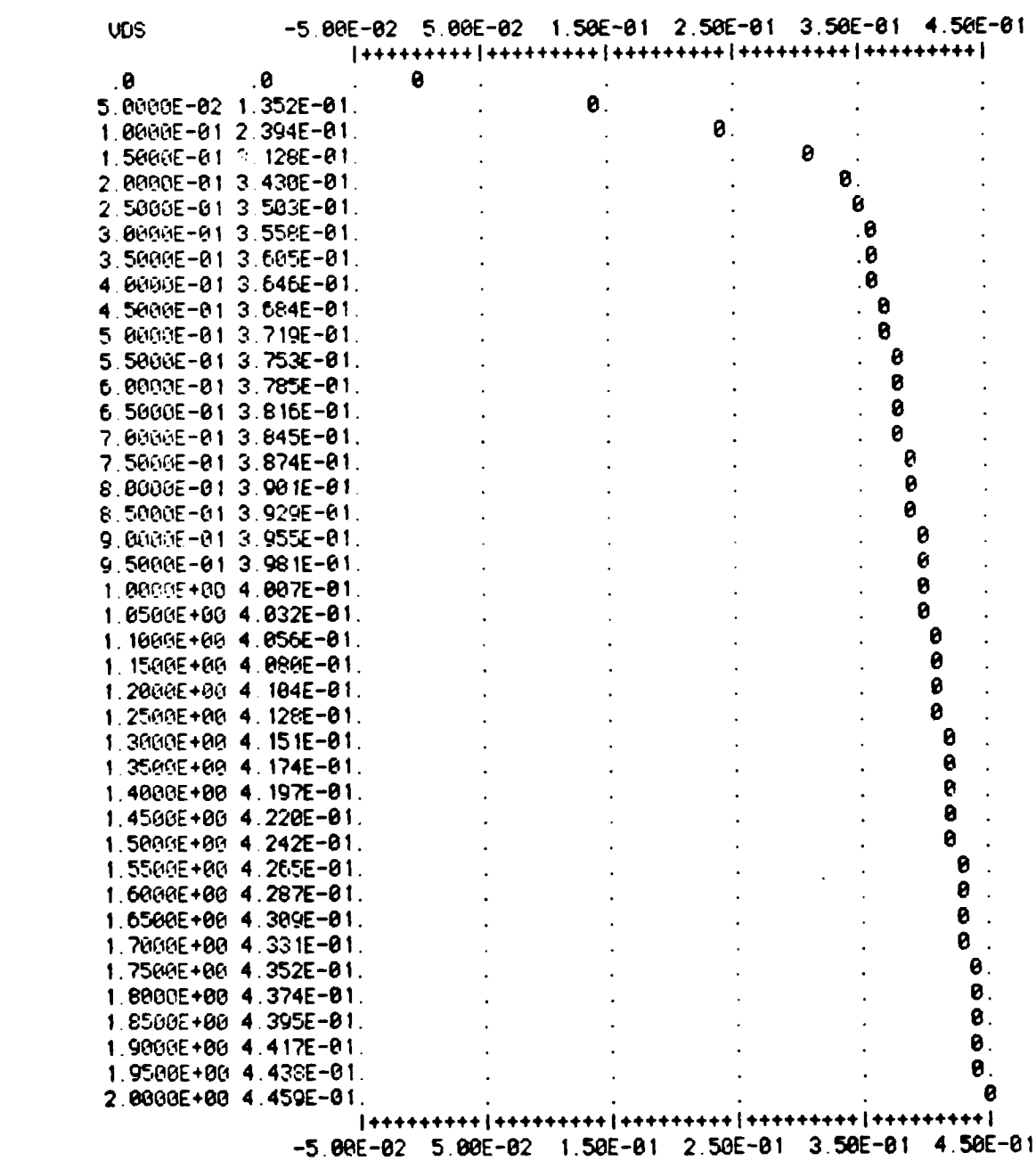
```
ENHANCEMENT (NORMALLY OFF) MESFET I-V CHARACTERISTIC: VGS = 0.6V
.PC NP REPRINT
.TFUN VDS 0.05V 0V 2V
.OUTPUT TFUN ID M1
.PARAM VDS=0V VGS=0.6V
M1 2 1 0 ENHMD 10 0.6 0V VGS
VINDS 2 0 DC VDS
VINGS 1 0 DC VGS
.MODEL ENHMD NMOS BULK=0 VT=0.15 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.END
```

MOSFET I-V CURVE WITH VGS = 0.6V

TEMPERATURE = 25.0

TRANSFER FUNCTION -

0) TFUN ID * 1.0E+03 M1



```
DEPLETION (NORMALLY ON) MESFET I-V CHARACTERISTIC: VGS = 0V
.PC NP REPRINT
.TFUN VDS 0.05V 0V 2V
.OUTPUT TFUN ID M1
.PARAM VDS=0V VGS=0V
M1 2 1 0 DEPMD 3 0.6 0V VGS
VINDS 2 0 DC VDS
VINGS 1 0 DC VGS
.MODEL DEPMD NMOS BULK=0 VT=-0.5 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.END
```

MOSFET I-V CURVE WITH VGS = 0V

TEMPERATURE = 25.0

TRANSFER FUNCTION -

0) TFUN ID * 1.0E+03 M1

```
  VDS            -2.00E-02  2.00E-02  6.00E-02  1.00E-01  1.40E-01  1.80E-01
                      |+++++++++|+++++++++|+++++++++|+++++++++|+++++++++|
   .0          .0          0
 5.0000E-02 4.560E-02.           .     0     .         .         .         .
 1.0000E-01 8.188E-02.           .           .  0      .         .         .
 1.5000E-01 1.089E-01.           .           .         .  0      .         .
 2.0000E-01 1.237E-01.           .           .         .     0   .         .
 2.5000E-01 1.267E-01.           .           .         .      0  .         .
 3.0000E-01 1.288E-01.           .           .         .      0  .         .
 3.5000E-01 1.306E-01.           .           .         .       0 .         .
 4.0000E-01 1.321E-01.           .           .         .       0 .         .
 4.5000E-01 1.335E-01.           .           .         .       0 .         .
 5.0000E-01 1.348E-01.           .           .         .        0.         .
 5.5000E-01 1.360E-01.           .           .         .        0.         .
 6.0000E-01 1.372E-01.           .           .         .        0.         .
 6.5000E-01 1.383E-01.           .           .         .         0         .
 7.0000E-01 1.394E-01.           .           .         .         0         .
 7.5000E-01 1.405E-01.           .           .         .         0         .
 8.0000E-01 1.415E-01.           .           .         .         0         .
 8.5000E-01 1.425E-01.           .           .         .          0        .
 9.0000E-01 1.434E-01.           .           .         .          0        .
 9.5000E-01 1.444E-01.           .           .         .          0        .
 1.0000E+00 1.453E-01.           .           .         .          0        .
 1.0500E+00 1.462E-01.           .           .         .           0       .
 1.1000E+00 1.471E-01.           .           .         .           0       .
 1.1500E+00 1.480E-01.           .           .         .           0       .
 1.2000E+00 1.489E-01.           .           .         .           0       .
 1.2500E+00 1.497E-01.           .           .         .           0       .
 1.3000E+00 1.506E-01.           .           .         .            0      .
 1.3500E+00 1.514E-01.           .           .         .            0      .
 1.4000E+00 1.523E-01.           .           .         .            0      .
 1.4500E+00 1.531E-01.           .           .         .            0      .
 1.5000E+00 1.539E-01.           .           .         .            0      .
 1.5500E+00 1.547E-01.           .           .         .             0     .
 1.6000E+00 1.555E-01.           .           .         .             0     .
 1.6500E+00 1.563E-01.           .           .         .             0     .
 1.7000E+00 1.571E-01.           .           .         .             0     .
 1.7500E+00 1.579E-01.           .           .         .             0     .
 1.8000E+00 1.587E-01.           .           .         .              0    .
 1.8500E+00 1.595E-01.           .           .         .              0    .
 1.9000E+00 1.602E-01.           .           .         .              0    .
 1.9500E+00 1.610E-01.           .           .         .              0    .
 2.0000E+00 1.618E-01.           .           .         .              0    .
                      |+++++++++|+++++++++|+++++++++|+++++++++|+++++++++|
                  -2.00E-02  2.00E-02  6.00E-02  1.00E-01  1.40E-01  1.80E-01
```

```
E TO D INVERTER TRANSFER FUNCTION
.PC NP REPRINT
.TFUN VIN 0.02 0V 0.8V
.OUTPUT TFUN VOUT 2 0
.PARAM VIN = 0V
M1 2 1 0 ENHMD 10 0.6
M2 3 2 2 DEPMD 3 0.6
VINP 1 0 DC VIN
VCC 3 0 DC 1V
.MODEL DEPMD NMOS BULK=0 VT=-0.5 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.MODEL ENHMD NMOS BULK=0 VT=0.15 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.END
```

E TO D INVERTER

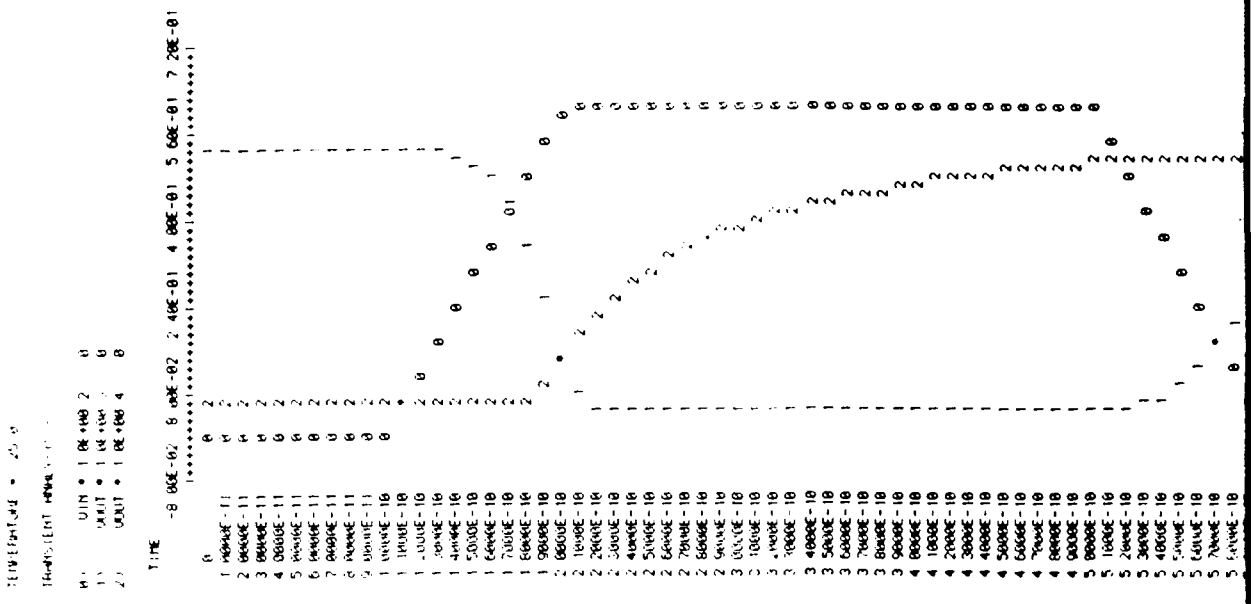
TEMPERATURE = 25.0

TRANSFER FUNCTION -

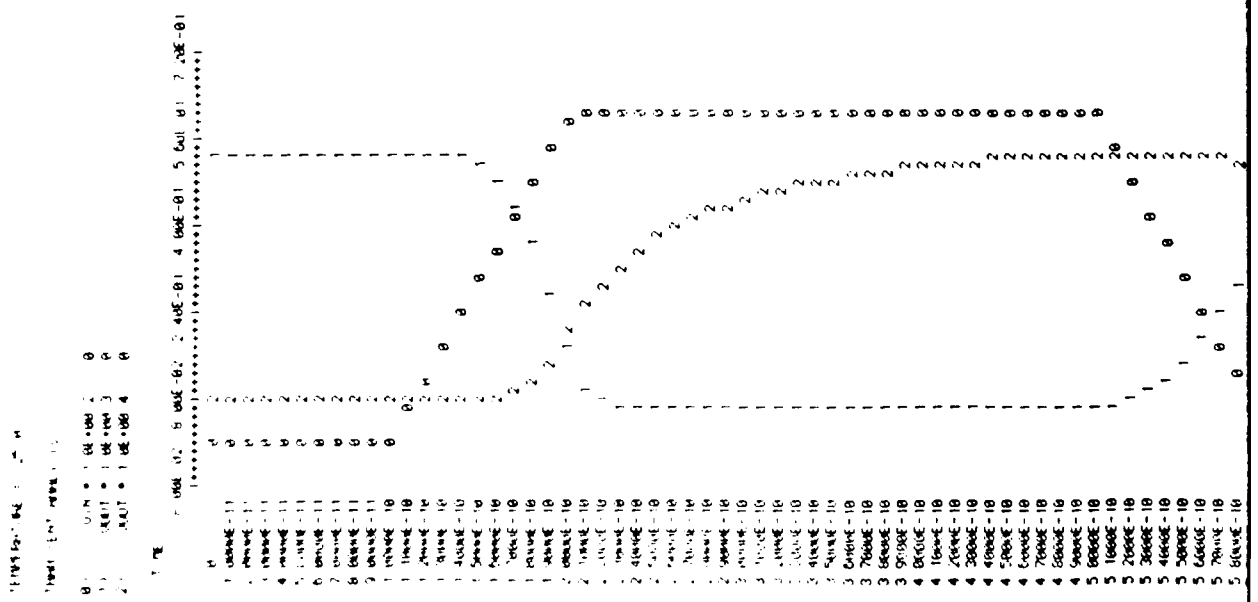
0) TFUN VOUT * 1.0E+00 2 0

```
 VIN            -8.00E-02  8.00E-02  2.40E-01  4.00E-01  5.60E-01  7.20E-01
                 |+++++++++|+++++++++|+++++++++|+++++++++|+++++++++|
  .0        6.674E-01.                                            0 .
 2.0000E-02 6.675E-01.                                            0 .
 4.0000E-02 6.676E-01.                                            0 .
 6.0000E-02 6.677E-01.                                            0 .
 8.0000E-02 6.677E-01.                                            0 .
 1.0000E-01 6.677E-01.                                            0 .
 1.2000E-01 6.677E-01.                                            0 .
 1.4000E-01 6.677E-01.                                            0 .
 1.6000E-01 6.409E-01.                                         0    .
 1.8000E-01 5.883E-01.                                      0       .
 2.0000E-01 5.369E-01.                                   0          .
 2.2000E-01 4.866E-01.                                0             .
 2.4000E-01 4.374E-01.                             0                .
 2.6000E-01 3.891E-01.                          0                   .
 2.8000E-01 3.418E-01.                       0                      .
 3.0000E-01 2.955E-01.                    0                         .
 3.2000E-01 2.504E-01.                 0                            .
 3.4000E-01 2.065E-01.              0                               .
 3.6000E-01 1.642E-01.           0                                  .
 3.8000E-01 1.245E-01.        0                                     .
 4.0000E-01 9.877E-02.       0                                      .
 4.2000E-01 8.665E-02.       0                                      .
 4.4000E-01 7.728E-02.       0                                      .
 4.6000E-01 7.059E-02.      0                                       .
 4.8000E-01 6.522E-02.      0                                       .
 5.0000E-01 6.076E-02.      0                                       .
 5.2000E-01 5.697E-02.      0                                       .
 5.4000E-01 5.369E-02.     0                                        .
 5.6000E-01 5.082E-02.     0                                        .
 5.8000E-01 4.827E-02.     0                                        .
 6.0000E-01 4.599E-02.     0                                        .
 6.2000E-01 4.393E-02.     0                                        .
 6.4000E-01 4.207E-02.     0                                        .
 6.6000E-01 4.037E-02.     0                                        .
 6.8000E-01 3.881E-02.    0                                         .
 7.0000E-01 3.738E-02.    0                                         .
 7.2000E-01 3.605E-02.    0                                         .
 7.4000E-01 3.482E-02.    0                                         .
 7.6000E-01 3.368E-02.    0                                         .
 7.8000E-01 3.261E-02.    0                                         .
 8.0000E-01 3.161E-02.    0                                         .
                 |+++++++++|+++++++++|+++++++++|+++++++++|+++++++++|
               -8.00E-02  8.00E-02  2.40E-01  4.00E-01  5.60E-01  7.20E-01
```

```
E TO D INVERTER TRANSIENT ANALYSIS (3 MICRON WIDE DMESFET)
.PC NP
.TRAN 10PS 1000PS
.PLOT VIN 2 0 VOUT 3 0 VOUT 4 0
MA1 3 2 0 ENHMD 10 0.6
MA2 1 3 3 DEPMD 3 0.6
DIA 2 0 DIODE
MB1 4 3 0 ENHMD 10 0.6
MB2 1 4 4 DEPMD 3 0.6
DIB 3 0 DIODE
MC1 5 4 0 ENHMD 10 0.6
MC2 1 5 5 DEPMD 3 0.6
DIC 4 0 DIODE
VINP 2 0 DC 0V PL 0V 100PS 0.6V 200PS 0.6V 500PS 0V 600PS
VCC 1 0 DC 1V
.MODEL DEPMD NMOS BULK=0 VT=-0.5 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.MODEL ENHMD NMOS BULK=0 VT=0.15 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.MODEL DIODE D IS=1E-14 CJA=10E-15 RS=100
.END
```

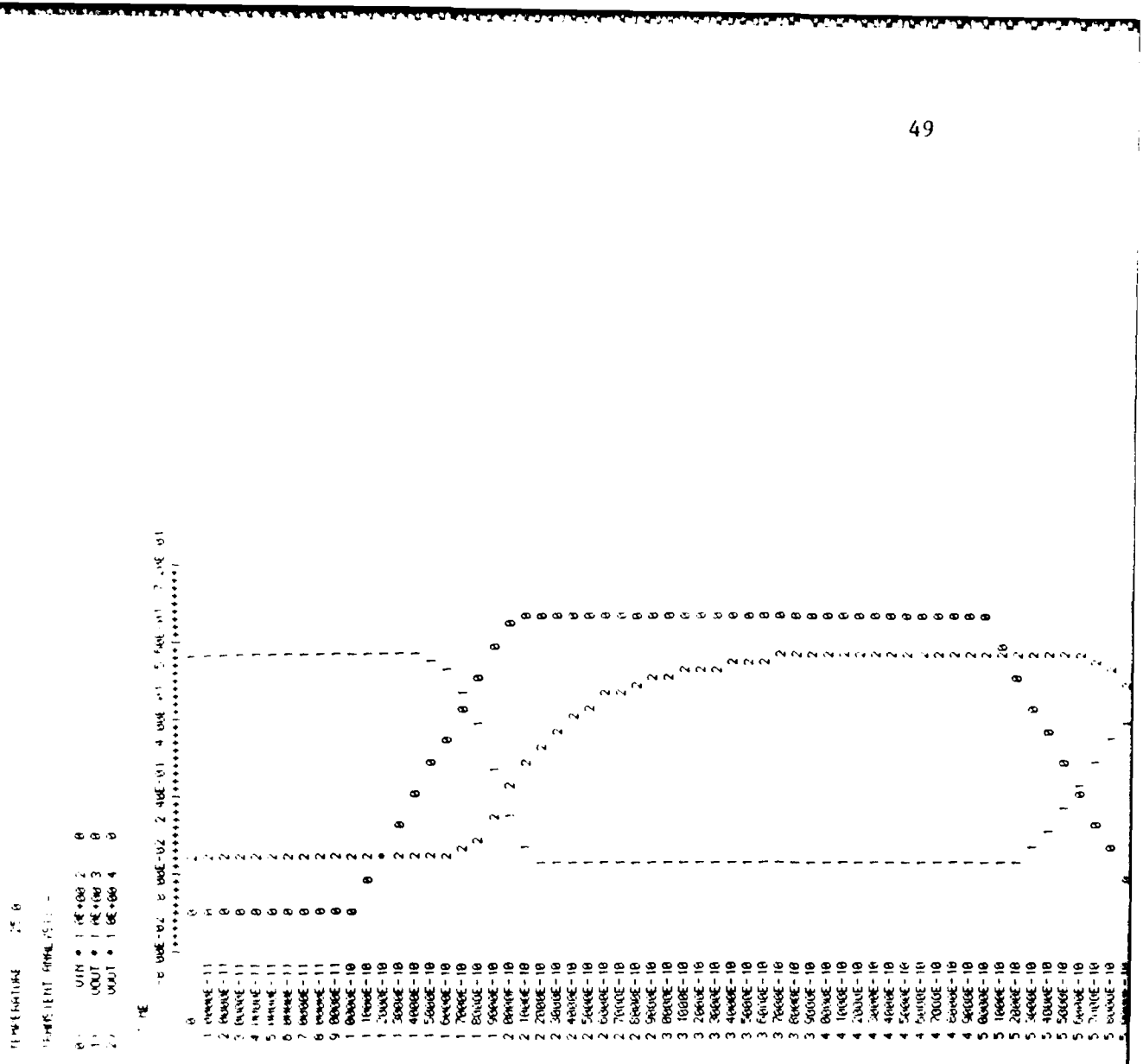


INVERTER TRANSIENT ANALYSIS WITH 3 MICRON WIDE (NORMAL) D-MESFET
VIN (0) = INPUT SIGNAL; VOUT (1) = NOT(VIN (0)); VOUT (2) = NOT(VOUT (1))



INVERTER TRANSIENT ANALYSIS WITH 4.5 MICRON WIDE D-MESFET

MESFET
= NOT(VOUT (1))

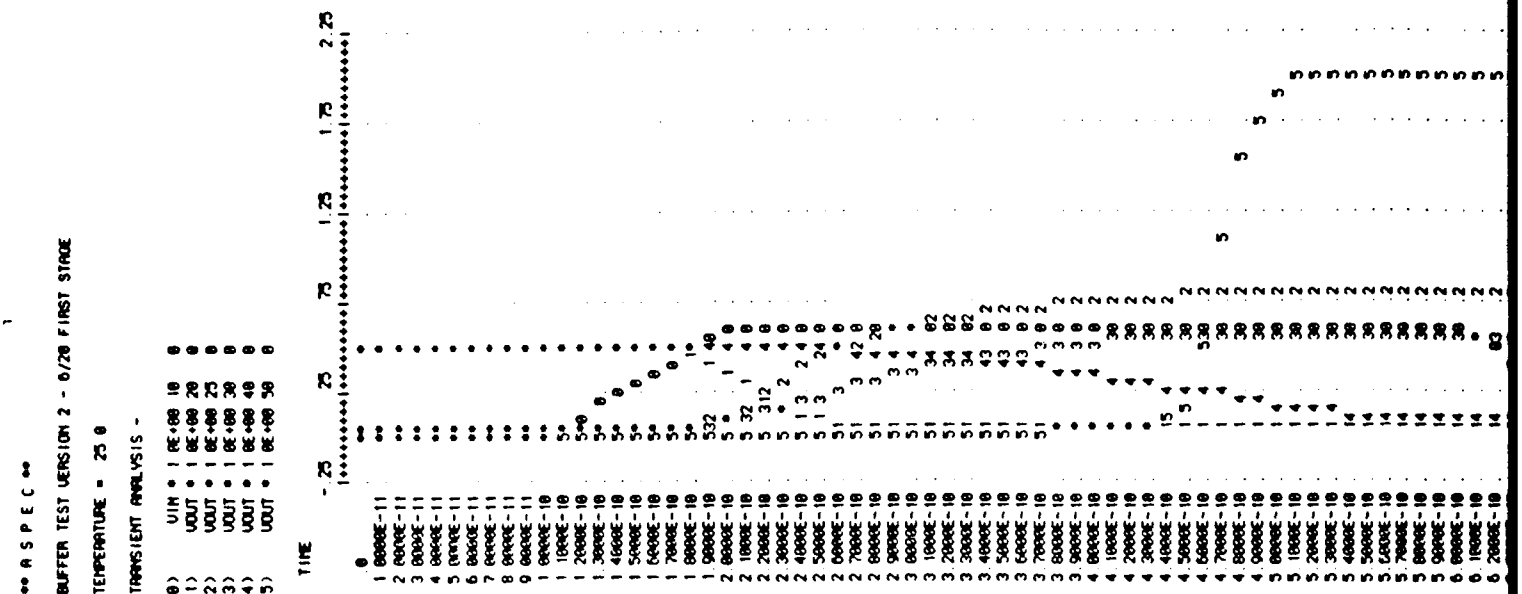


INVERTER TRANSIENT ANALYSIS WITH 6 MICRON WIDE D-MESFET

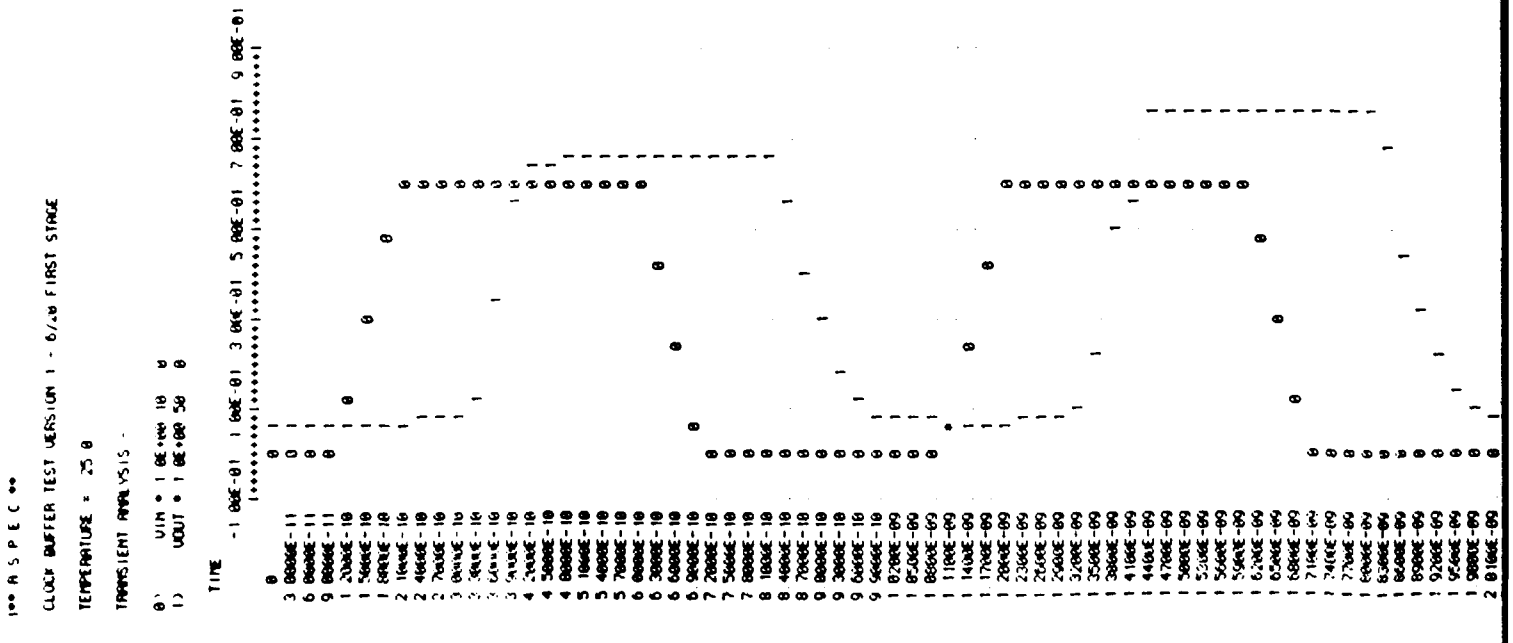
ET

```
COAXIAL CABLE LINE DRIVER - TRANSIENT ANALYSIS
.TRAN 10PS 1200PS
.PLOT VIN 10 0 VOUT 20 0 VOUT 25 0 VOUT 30 0 VOUT 40 0 VOUT 50 0
$ INVERTER A
MA1 20 10 0 ENHMD 20 0.6
MA2 1 20 20 DEPMD 6 0.6
DIA 10 0 DIODE 2
$ INVERTER B
MB1 25 20 0 ENHMD 10 0.6
MB2 1 25 25 DEPMD 3 0.6
DIB 20 0 DIODE
$ INVERTER C
MC1 30 20 0 ENHMD 20 0.6
DEC 20 0 DIODE 2
MC2 1 25 30 DEPMD 6 0.6
DDC 25 30 DIODE 0.6
$ STAGE D
MD1 40 30 0 ENHMD 70 0.6
MD2 1 20 40 DEPMD 30 0.6
DED 30 0 DIODE 7
DDD 20 40 DIODE 3
$ FINAL STAGE
ME1 50 40 0 ENHMD 500 0.6
DEE 40 0 DIODE 50
RPULLUP 1 50 1K
$ ----
VINP 10 0 DC 0V PL 0V 100PS 0.6V 200PS 0.6V 600PS 0V 700PS
VCC 1 0 DC 2V
.MODEL DEPMD NMOS BULK=0 VT=-0.5 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.MODEL ENHMD NMOS BULK=0 VT=0.15 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.MODEL DIODE D IS=1E-14 CJA=10E-15 RS=100
.END
```

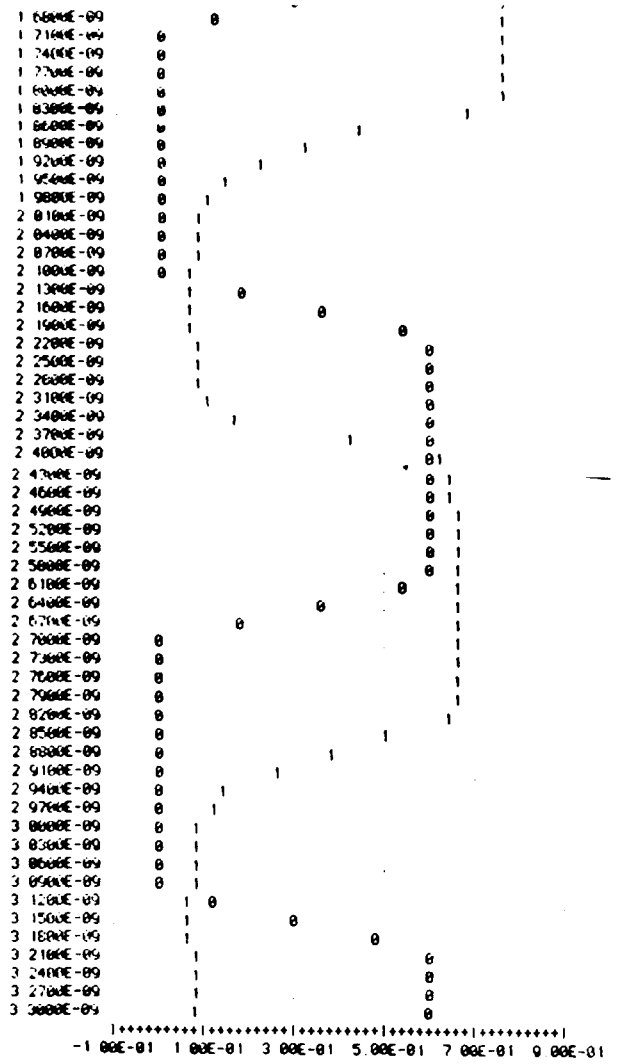
```
OUTPUT BUFFER - TRANSIENT ANALYSIS
.TRAN 30PS 3300PS
.PLOT VIN 10 0 VOUT 50 0
$ INVERTER A
MA1 20 10 0 ENHMD 20 0.6
MA2 1 20 20 DEPMD 6 0.6
DIA 10 0 DIODE 2
$ INVERTER B
MB1 25 20 0 ENHMD 10 0.6
MB2 1 25 25 DEPMD 3 0.6
DIB 20 0 DIODE
$ INVERTER C
MC1 30 20 0 ENHMD 20 0.6
DEC 20 0 DIODE 2
MC2 1 25 30 DEPMD 6 0.6
DDC 25 30 DIODE 0.6
$ STAGE D
MD1 40 30 0 ENHMD 70 0.6
MD2 1 20 40 DEPMD 30 0.6
DED 30 0 DIODE 7
DDD 20 40 DIODE 3
$ FINAL STAGE
ME1 50 40 0 ENHMD 200 0.6
ME2 1 50 50 DEPMD 60 0.6
DEE 40 0 DIODE 20
$ ----
VINP 10 0 DC 0V PL 0V 100PS 0.6V 200PS 0.6V 600PS 0V 700PS 0V 1100PS R 100PS
VCC 1 0 DC 2V
.MODEL DEPMD NMOS BULK=0 VT=-0.5 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.MODEL ENHMD NMOS BULK=0 VT=0.15 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.MODEL DIODE D IS=1E-14 CJA=10E-15 RS=100
.END
```

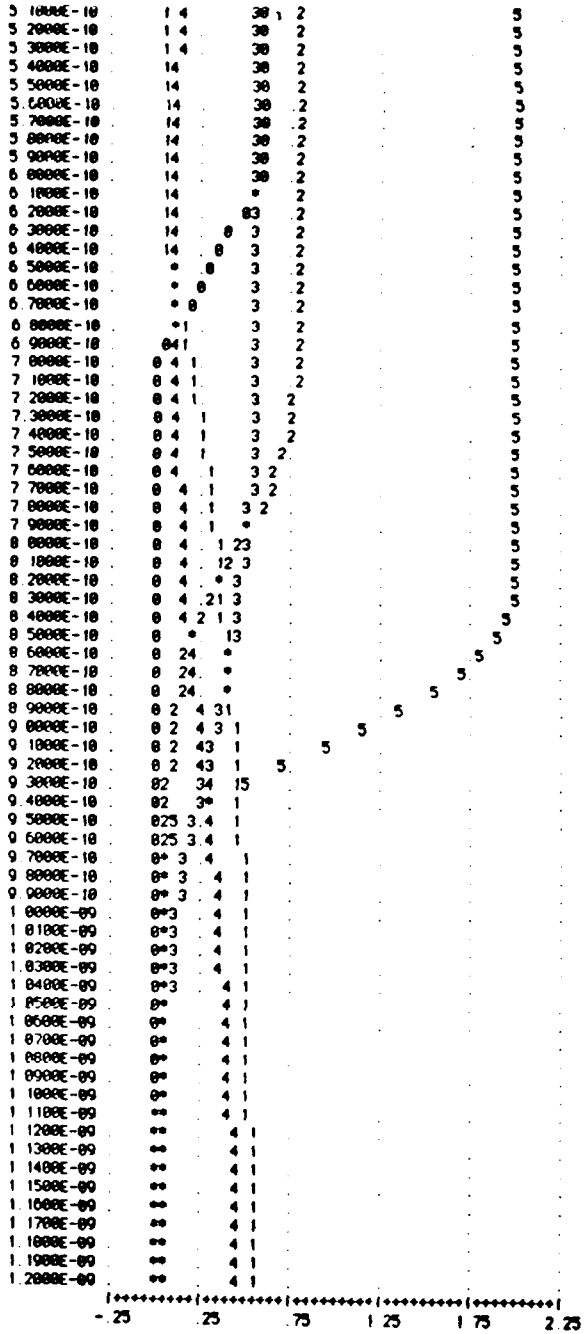


COAXIAL CABLE LINE DRIVER TRANSIENT ANALYSIS -
VIN (0) = INPUT SIGNAL; VOUT (5) = FINAL AMPLIFIED OUTPUT (FROM 500 MICRON E-MESFET); PROPAGATION DELAY = 320 ps APPROX.

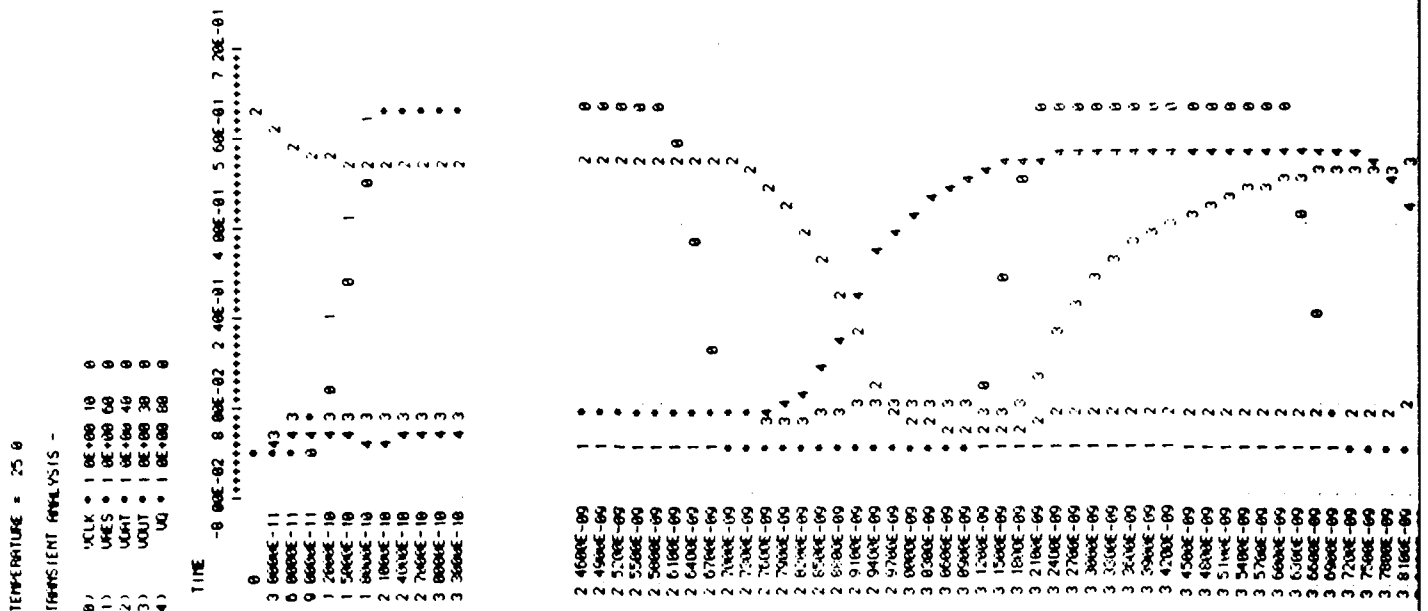


OUTPUT BUFFER TRANSIENT ANALYSIS -
VIN (0) = INPUT SIGNAL; VOUT (1) = FINAL AMPLIFIED OUTPUT;
PROPAGATION DELAY = 220 ps APPROX.

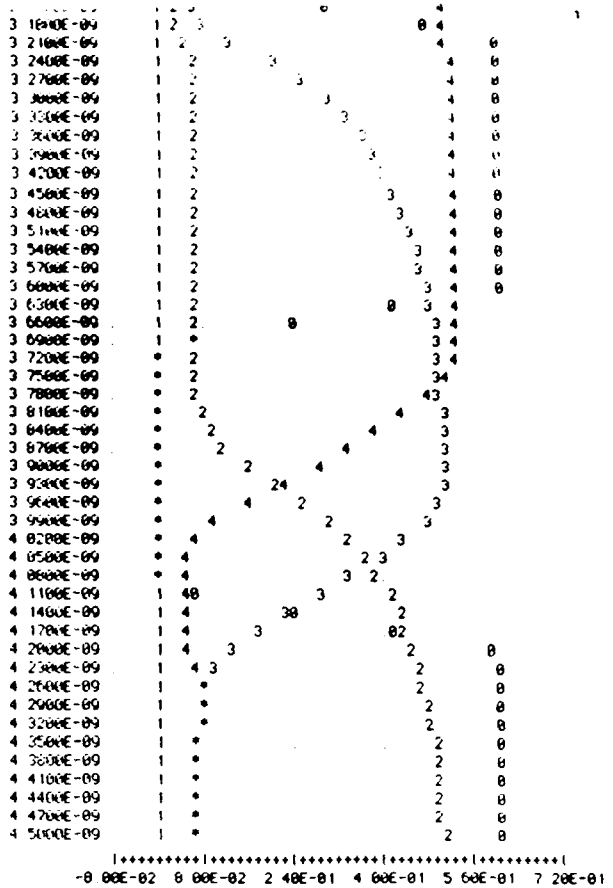

-1.00E-01
1.00E-01
3.00E-01
5.00E-01
7.00E-01
9.00E-01

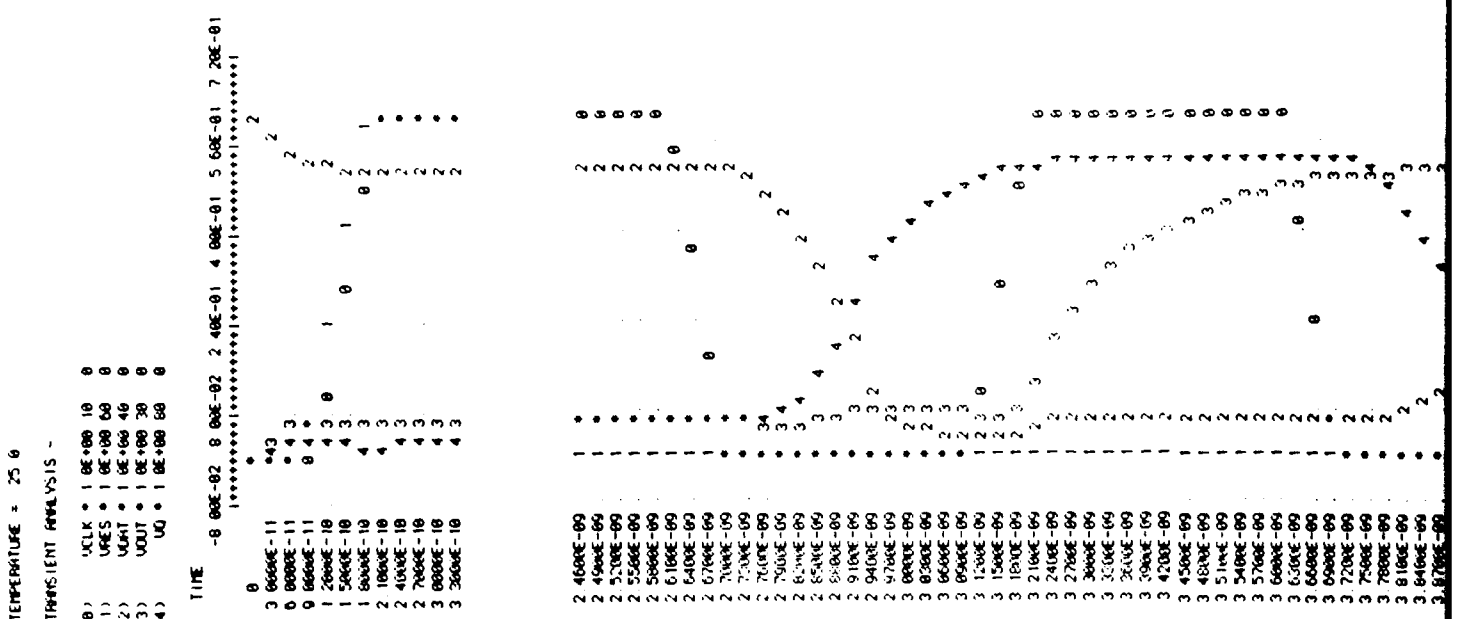

-.25
.25
.75
1.25
1.75
2.25

```
D FLIP-FLOP PROPAGATION DELAY ANALYSIS
.PC NP
.TRAN 30PS 4500PS
.PLOT VCLK 10 0 VRES 60 0 VDAT 40 0 VOUT 30 0 VQ 80 0
.DCVOLT 80 0V 40 0.6V 50 0V 70 0.6V 20 0V 30 0V
$ MACRO DEFINITION
.MACRO NOR3 1 2 3 4 5 6
ME1 5 2 6 ENHMD 10 0.6
D1 2 6 DIODE
ME2 5 3 6 ENHMD 10 0.6
D2 3 6 DIODE
ME3 5 4 6 ENHMD 10 0.6
D3 4 6 DIODE
MD1 1 5 5 DEPMD 3 0.6
.EOM
.MODEL DEPMD NMOS BULK=0 VT=-0.5 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.MODEL ENHMD NMOS BULK=0 VT=0.15 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.MODEL DIODE D IS=1E-14 CJA=10E-15 RS=100
$ MACRO EXPANSIONS
XAA 100 60 30 70 50 0 NOR3
XA 100 50 0 10 70 0 NOR3
XB 100 70 10 30 20 0 NOR3
XBB 100 20 0 40 30 0 NOR3
XQ 100 60 70 40 80 0 NOR3
XQB 100 80 20 0 40 0 NOR3
VCLK 10 0 DC 0V PL 0V 100PS 0.6V 200PS 0.6V 600PS 0V 700PS
+ 0V 1100PS R 100PS
VRESET 60 0 DC 0V PL 0V 80PS 0.6V 180PS 0.6V 1980PS 0V 2080PS
VCC 100 0 DC 2V
.END
```



D FLIP-FLOP PROPAGATION DELAY ANALYSIS -
(0) = CLOCK SIGNAL
(1) = RESET SIGNAL
(2) = D INPUT SIGNAL ($\overline{Q}$ OUTPUT OF THE FLIP-FLOP)
(4) = Q OUTPUT OF THE FLIP-FLOP


-0 00E-02
0 00E-02
2 40E-01
4 00E-01
5 60E-01
7 20E-01



D FLIP-FLOP PROPAGATION DELAY ANALYSIS -
(0) = CLOCK SIGNAL
(1) = RESET SIGNAL
(2) = D INPUT SIGNAL ($\overline{Q}$ OUTPUT OF THE FLIP-FLOP)
(4) = Q OUTPUT OF THE FLIP-FLOP

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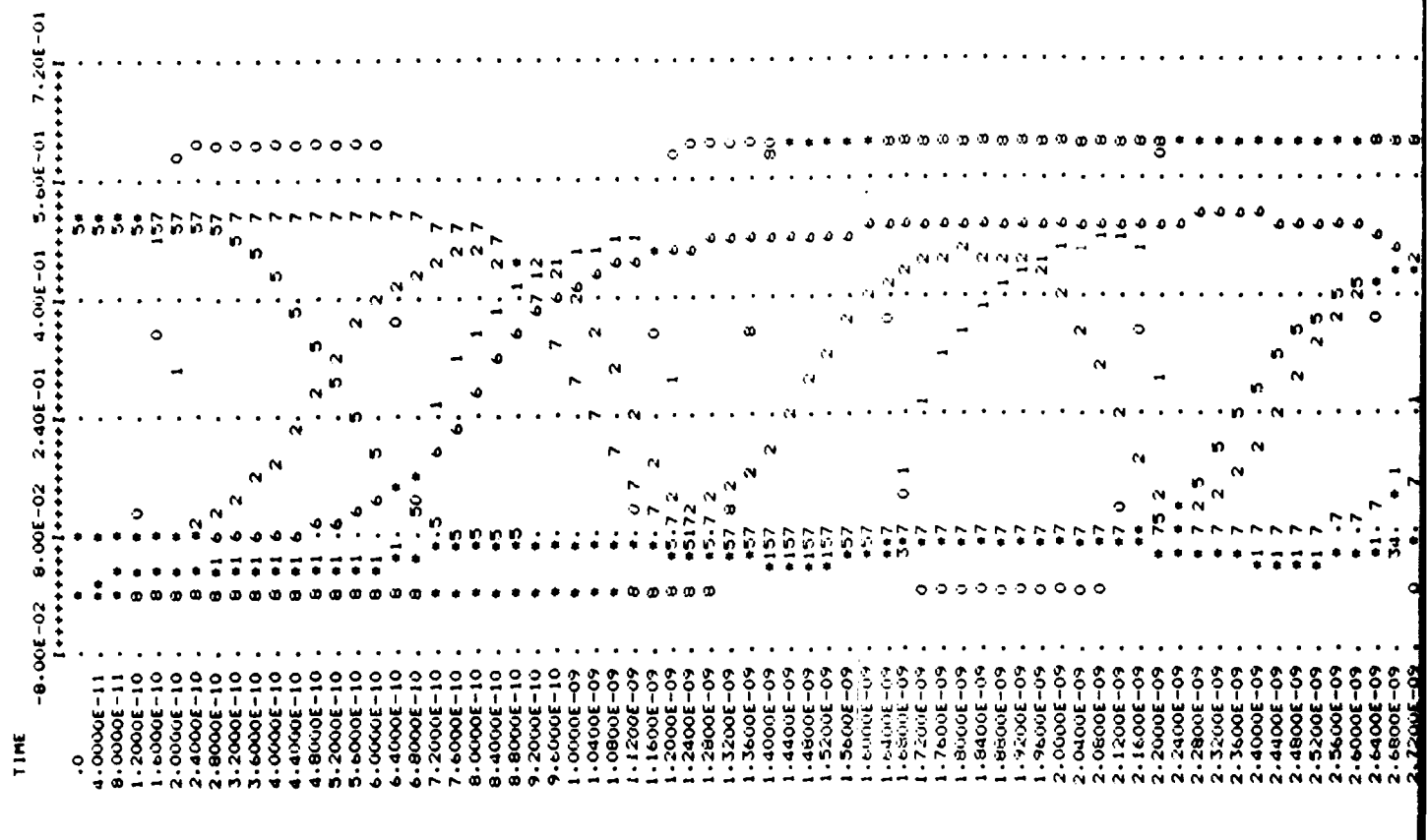
```
TRANSMITTER MODEL-REDUCED TEST FILE
.PC NP
.TRAN 40PS 5.7NS
.PLOT VCLK 2 0 VNCLK 63 0 VCLKD 64 0 VQ1 61 0 VSRO 62 0 VOFL1 49 0
+ VLOAD 50 0 VSHFT 80 0 VI1 53 0
.PLOT VCLK 2 0 VBLS1 55 0 VBLP1 56 0 VBLS0 57 0 VBLP0 58 0 VBLN1 59 0
+ VBLN0 60 0 VQA 17 0 VQB 26 0 VQC 35 0 VQD 43 0
$ MACRO DEFINITION ////////////////////
.MACRO DFFFET 0 1 2 3 4 11 5 6
$ ------ NOR GATE AA
MAA1 7 4 0 ENHMD 10 0.6
DAA1 4 0 DIODE
MAA2 7 10 0 ENHMD 10 0.6
DAA2 10 0 DIODE
MAA3 7 8 0 ENHMD 10 0.6
DAA3 8 0 DIODE
MAAD 1 7 7 DEPMD 3 0.6
$ ------ NOR GATE A
MA1 8 7 0 ENHMD 10 0.6
DA1 7 0 DIODE
MA2 8 11 0 ENHMD 10 0.6
DA2 11 0 DIODE
MA3 8 2 0 ENHMD 10 0.6
DA3 2 0 DIODE
MAD 1 8 8 DEPMD 3 0.6
$ ------ NOR GATE B
MB1 9 8 0 ENHMD 10 0.6
DB1 8 0 DIODE
MB2 9 2 0 ENHMD 10 0.6
DB2 2 0 DIODE
MB3 9 10 0 ENHMD 10 0.6
DB3 10 0 DIODE
MBD 1 9 9 DEPMD 3 0.6
$ ------ NOR GATE BB
MBB1 10 9 0 ENHMD 10 0.6
DBB1 9 0 DIODE
MBB2 10 11 0 ENHMD 10 0.6
DBB2 11 0 DIODE
MBB3 10 3 0 ENHMD 10 0.6
DBB3 3 0 DIODE
MBBD 1 10 10 DEPMD 3 0.6
$ ------ NOR GATE Q
MQ1 5 4 0 ENHMD 10 0.6
DQ1 4 0 DIODE
MQ2 5 8 0 ENHMD 10 0.6
DQ2 8 0 DIODE
MQ3 5 6 0 ENHMD 10 0.6
DQ3 6 0 DIODE
MQD 1 5 5 DEPMD 3 0.6
$ ------ NOR GATE QB
MQB1 6 5 0 ENHMD 10 0.6
DQB1 5 0 DIODE
MQB2 6 9 0 ENHMD 10 0.6
DQB2 9 0 DIODE
```

```
MQB3 6 11 0 ENHMD 10 0.6
DQB3 11 0 DIODE
MQBD 1 6 6 DEPMD 3 0.6
.DCVOLT 5 0V 6 0.6V 7 0V 8 0.6V 9 0V 10 0V
.EOM
$ ======================================
.MACRO NOT 0 1 2 3
ME1 3 2 0 ENHMD 10 0.6
D1 2 0 DIODE
MD 1 3 3 DEPMD 3 0.6
.EOM
$ ======================================
.MACRO NOR2 0 1 2 3 4
ME1 4 2 0 ENHMD 10 0.6
D1 2 0 DIODE
ME2 4 3 0 ENHMD 10 0.6
D2 3 0 DIODE
MD 1 4 4 DEPMD 3 0.6
.EOM
$ ======================================
.MACRO NOR3 0 1 2 3 4 5
ME1 5 2 0 ENHMD 10 0.6
D1 2 0 DIODE
ME2 5 3 0 ENHMD 10 0.6
D2 3 0 DIODE
ME3 5 4 0 ENHMD 10 0.6
D3 4 0 DIODE
MD 1 5 5 DEPMD 3 0.6
.EOM
$ ======================================
.MACRO NOR4 0 1 2 3 4 5 6
ME1 6 2 0 ENHMD 10 0.6
D1 2 0 DIODE
ME2 6 3 0 ENHMD 10 0.6
D2 3 0 DIODE
ME3 6 4 0 ENHMD 10 0.6
D3 4 0 DIODE
ME4 6 5 0 ENHMD 10 0.6
D3 5 0 DIODE
MD 1 6 6 DEPMD 3 0.6
.EOM
$ ======================================
.MACRO BUFFER 0 1 2 6
$ STAGE A
MA1 3 2 0 ENHMD 20 0.6
DIA 2 0 DIODE 2
MA2 1 3 3 DEPMD 6 0.6
$ STAGE B
MB1 4 3 0 ENHMD 10 0.6
DIB 3 0 DIODE
MB2 1 4 4 DEPMD 3 0.6
$ STAGE C
MC1 5 3 0 ENHMD 20 0.6
DEC 3 0 DIODE 2
```

```
MC2 1 4 5 DEPMD 6 0.6
DDC 4 5 DIODE 0.6
$ STAGE D
MD1 6 5 0 ENHMD 70 0.6
DED 5 0 DIODE 7
MD2 1 3 6 DEPMD 30 0.6
DDD 3 6 DIODE 3
.EOM
$ MACRO EXPANSIONS //////////////////////
$ === SEGMENT A ========================
XDFFA 0 1 2 11 51 0 12 13 DFFFET
XNGA1 0 1 12 14 NOT
XNGA2 0 1 12 15 NOT
XPSA1 0 1 13 16 NOT
XPSA2 0 1 13 17 NOT
XAS11 0 1 26 33 42 18 NOR3
XAS12 0 1 17 43 20 NOR2
XAS13 0 1 17 35 19 NOR2
XAS20 0 1 18 19 20 11 NOR3
$ === SEGMENT B ========================
XDFFB 0 1 2 21 51 0 22 23 DFFFET
XNGB1 0 1 22 24 NOT
XPSB1 0 1 23 25 NOT
XPSB2 0 1 23 26 NOT
XBS11 0 1 26 33 27 NOR2
XBS12 0 1 25 44 29 NOR2
XBS13 0 1 15 35 42 28 NOR3
XBS20 0 1 27 28 29 21 NOR3
$ === SEGMENT C ========================
XDFFC 0 1 2 30 0 52 31 32 DFFFET
XNGC1 0 1 31 33 NOT
XNGC2 0 1 31 33 NOT
XPSC1 0 1 32 34 NOT
XPSC2 0 1 32 35 NOT
XCS11 0 1 34 42 36 NOR2
XCS12 0 1 15 24 44 37 NOR3
XCS13 0 1 16 25 44 38 NOR3
XCS20 0 1 36 37 38 30 NOR3
$ === SEGMENT D ========================
XDFFD 0 1 2 39 51 0 40 41 DFFFET
XNGD1 0 1 40 42 NOT
XPSD1 0 1 41 43 NOT
XPSD2 0 1 41 44 NOT
XDS11 0 1 14 24 33 47 NOR3
XDS12 0 1 16 25 33 45 NOR3
XDS13 0 1 14 25 34 48 NOR3
XDS14 0 1 16 24 34 46 NOR3
XDS20 0 1 45 46 47 48 39 NOR4
$ === OUTPUT LOGIC =====================
XOFL1 0 1 17 26 35 43 49 NOR4
XNOFL 0 1 49 79 NOT
XLDBF 0 1 49 50 BUFFER
XSFBF 0 1 79 80 BUFFER
$ === SHIFT REGISTER ====================
```

```
XCNOT 0 1 2 63 NOT
XCBFR 0 1 63 64 BUFFER
$ --- SIMULATION OF ADDL LOAD ON BUFFER ---
MSRG1 65 64 0 ENHMD 120 7.2
DSRG1 64 0 DIODE 12
MSRG2 65 0 0 ENHMD 240 14.4
MSRGD 1 65 65 DEPMD 36 7.2
$ =======
XBLS1 0 1 0 80 55 NOR2
XBLP1 0 1 53 50 56 NOR2
XBLN1 0 1 55 56 59 NOR2
XBLK1 0 1 64 59 0 0 61 71 DFFFET
$ =======
XBLS0 0 1 61 80 57 NOR2
XBLP0 0 1 0 50 58 NOR2
XBLN0 0 1 57 58 60 NOR2
XBLK0 0 1 64 60 0 0 62 72 DFFFET
$ --- SIMULATION OF ADDL LOAD ON STMACH OUTPUTS ---
$ --- SIM LOAD ON LD ---
MLDLD1 67 50 0 ENHMD 140 8.4
DLDLD1 50 0 DIODE 14
MLDLD2 67 0 0 ENHMD 140 8.4
DLDLD2 0 0 DIODE 14
MLDLDD 1 67 67 DEPMD 42 8.4
$ --- SIM LOAD ON SHFT ---
MSFLD1 66 80 0 ENHMD 140 8.4
DSFLD1 80 0 DIODE 14
MSFLD2 66 0 0 ENHMD 140 8.4
DSFLD2 0 0 DIODE 14
MSFLDD 1 66 66 DEPMD 42 8.4
$ ///// MODEL PARAMETERS /////
.MODEL DEPMD NMOS BULK=0 VT=-0.5 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.MODEL ENHMD NMOS BULK=0 VT=0.15 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.MODEL DIODE D IS=1E-14 CJA=10E-15 RS=100
$ ********************************************************
VCLK 2 0 DC 0V PL 0V 100PS 0.6V 200PS 0.6V 600PS 0V 700PS
+ 0V 1100PS R 100PS
VRESET 51 0 DC 0V PL 0V 80PS 0.6V 180PS 0.6V 900PS 0V 1000PS
VSET 52 0 DC 0V PL 0V 80PS 0.6V 180PS 0.6V 900PS 0V 1000PS
VI1 53 0 DC 0V PL 0V 1300PS 0.6V 1400PS 0.6V 4400PS 0V 4500PS
VCC 1 0 DC 2V
.END
```



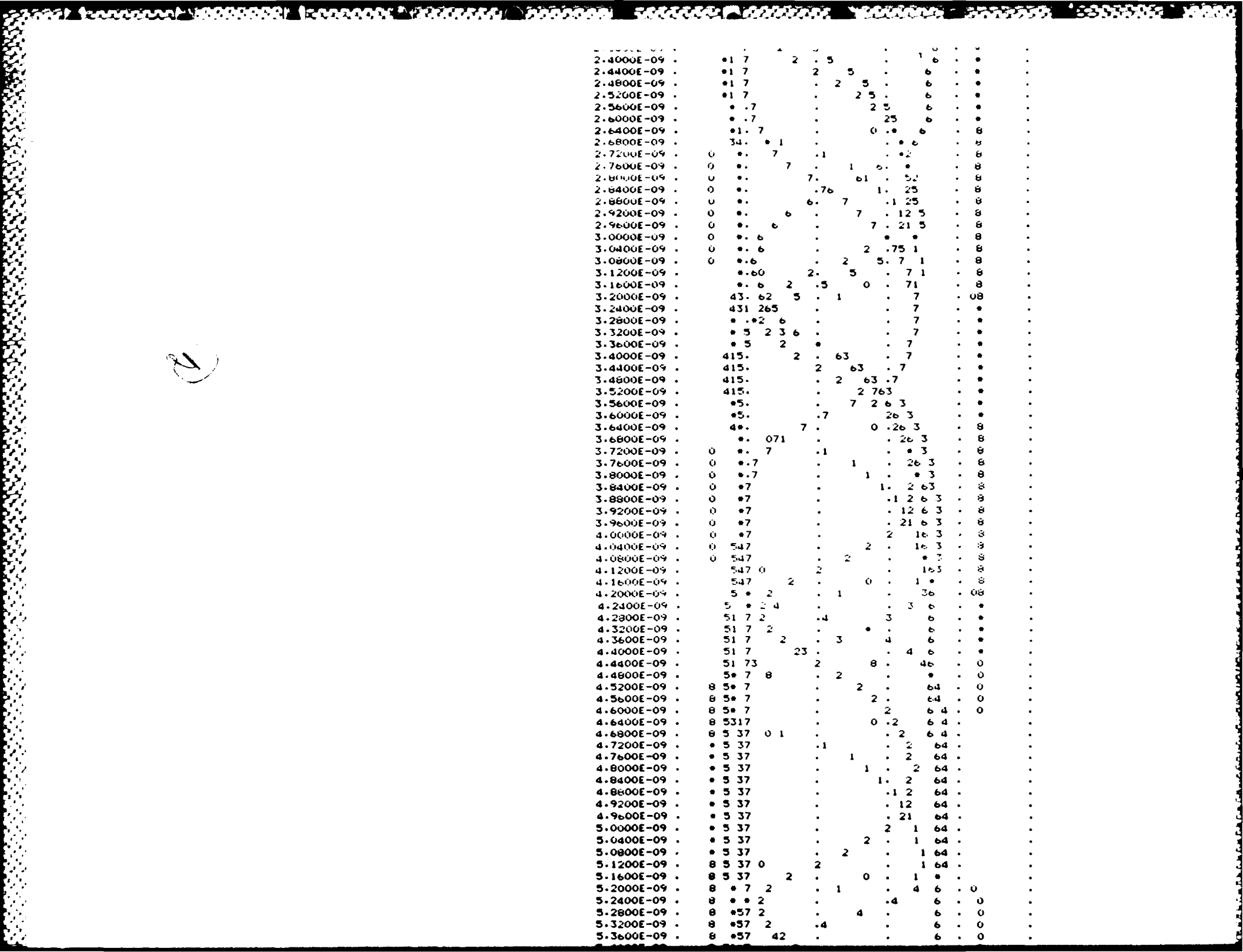
1** A S P E C **

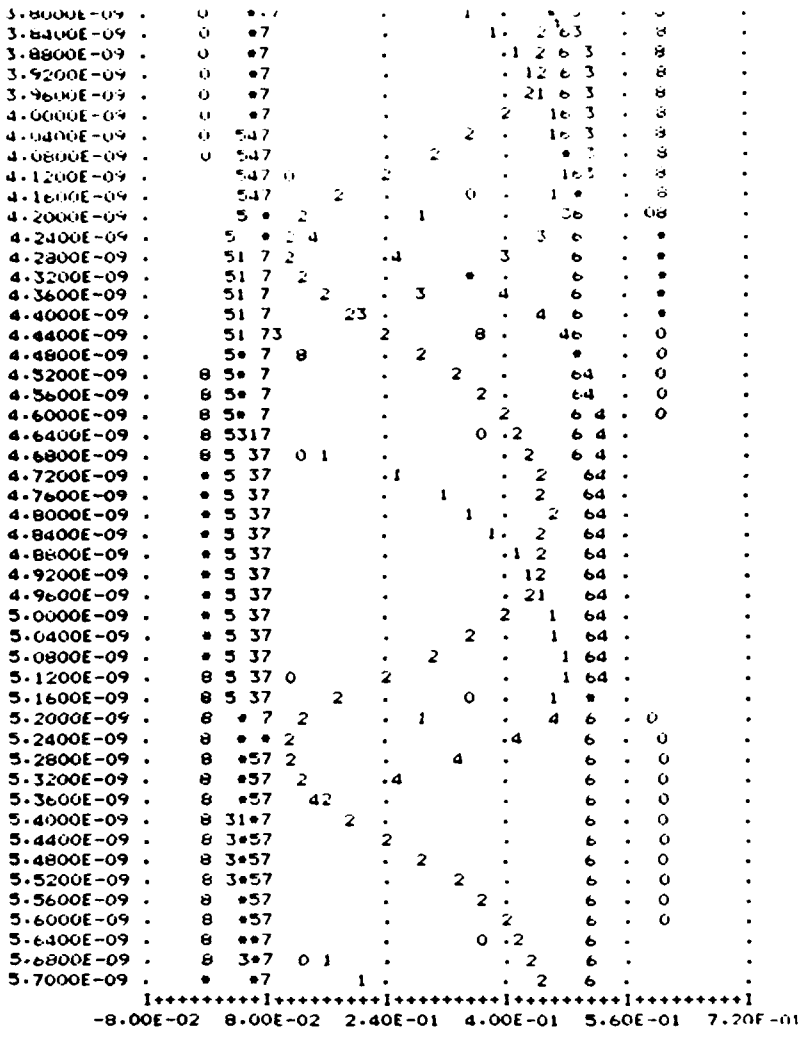
TRANSMITTER MODEL-REDUCED TEST FILE

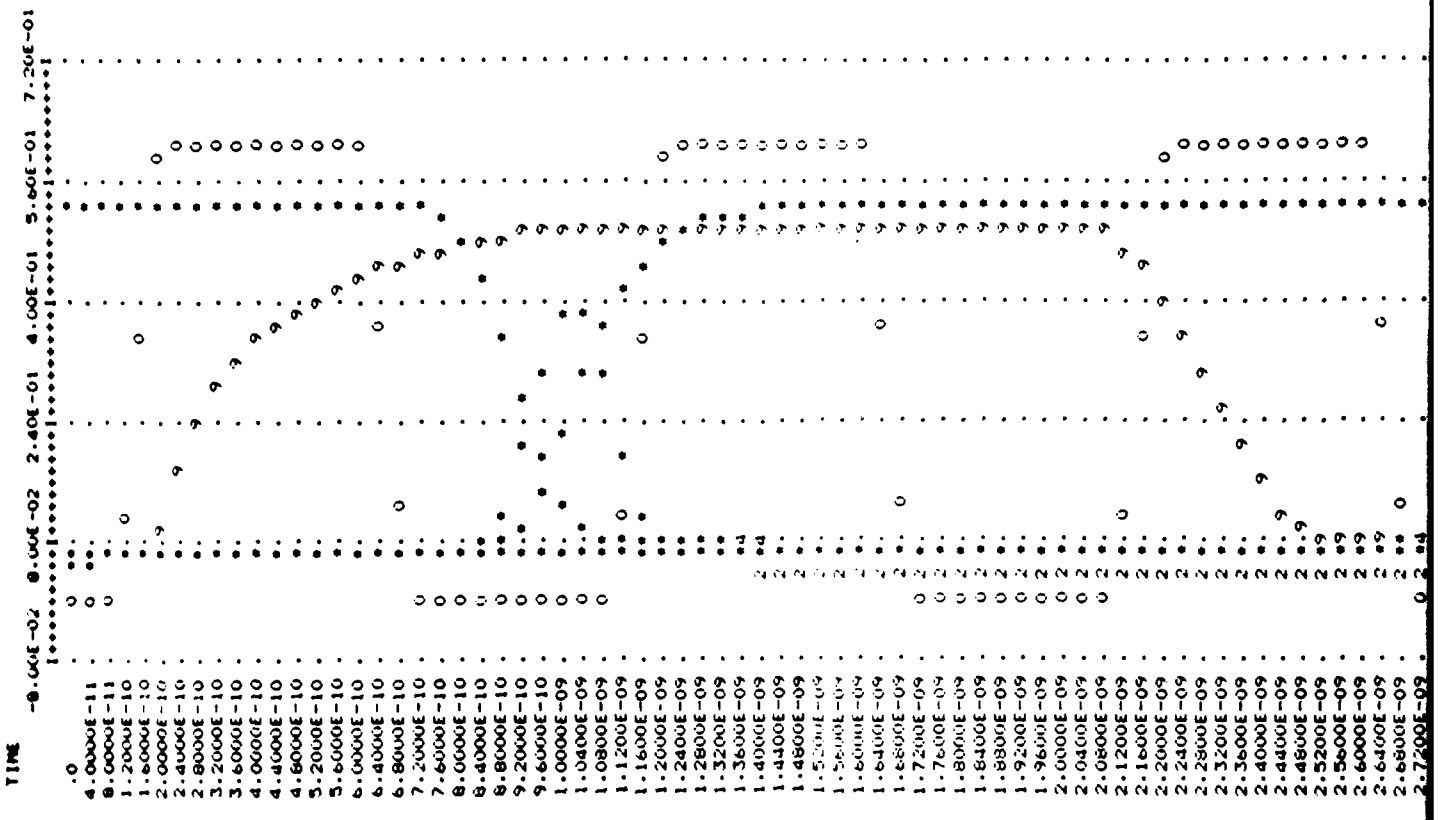
TEMPERATURE = 25.0

TRANSIENT ANALYSIS -

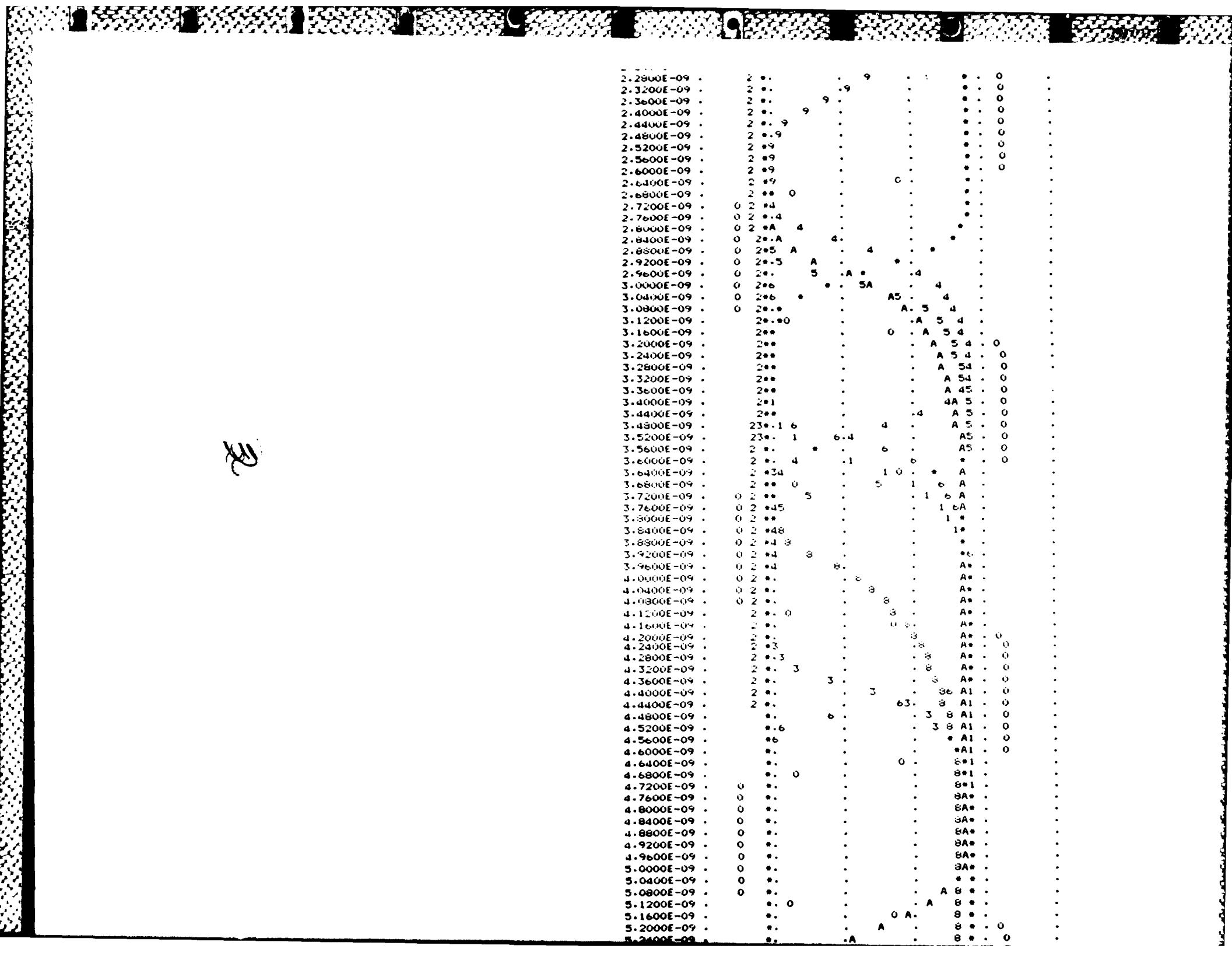
0) VCLK * 1.0E+00 2 0
1) VNCLK * 1.0E+00 63 0
2) VCLKD * 1.0E+00 64 0
3) VO1 * 1.0E+00 61 0
4) VSRO * 1.0E+00 62 0
5) VOFL1 * 1.0E+00 49 0
6) VLOAD * 1.0E+00 50 0
7) VSHFT * 1.0E+00 80 0
8) VI1 * 1.0E+00 53 0

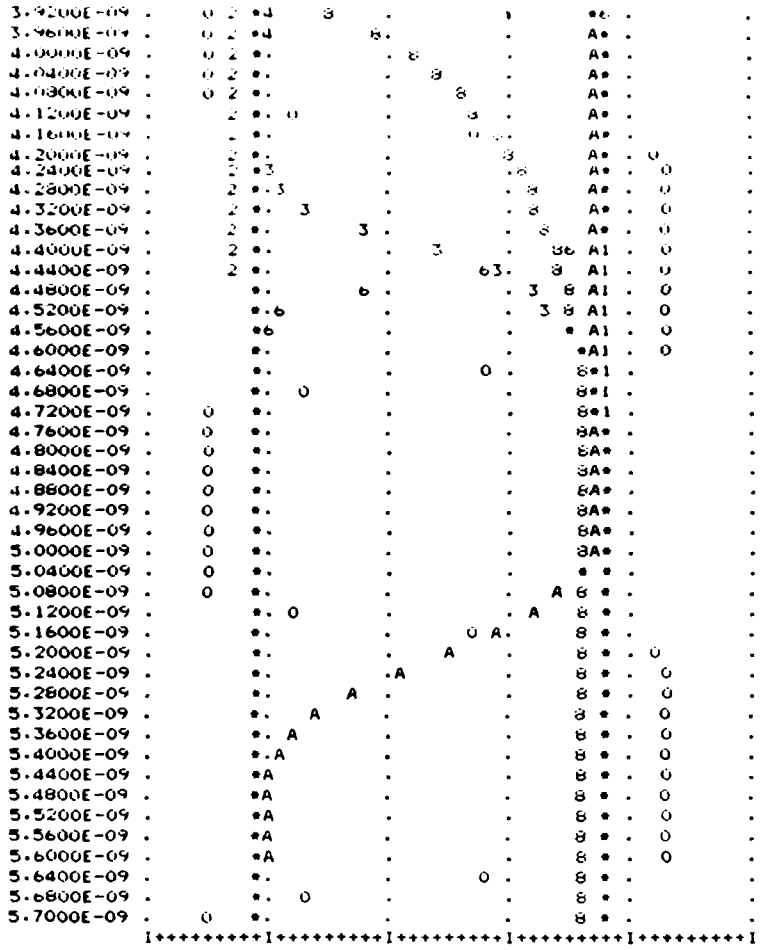



-8.00E-02
8.00E-02
2.40E-01
4.00E-01
5.60E-01
7.20E-01




```
1** A S P E C **

TRANSMITTER MODEL-REDUCED TEST FILE

TEMPERATURE =  25.0

TRANSIENT ANALYSIS -

0)      VCLK * 1.0E+00 2     0
1)     VBLS1 * 1.0E+00 55    0
2)     VBLP1 * 1.0E+00 56    0
3)     VBLS0 * 1.0E+00 57    0
4)     VBLP0 * 1.0E+00 58    0
5)     VBLN1 * 1.0E+00 59    0
6)     VBLN0 * 1.0E+00 60    0
7)       VOA * 1.0E+00 17    0
8)       VOB * 1.0E+00 26    0
9)       VOC * 1.0E+00 35    0
A)       VOD * 1.0E+00 43    0
```





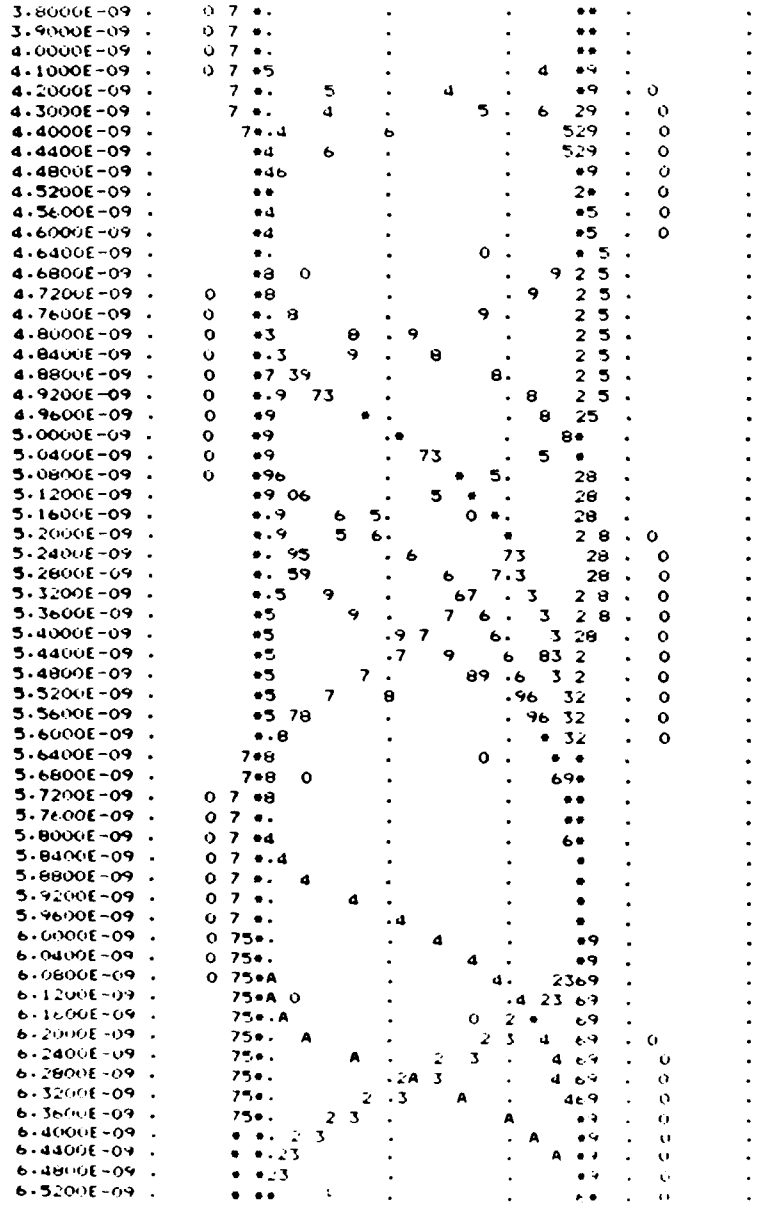
```
RECEIVER MODEL-REDUCED TEST FILE
.PC NP
.TRAN 100PS 4.4NS 40PS 6.8NS 100PS 8.2NS 40PS 9.7NS
.PLOT VCLK 2 0 VQA 17 0 VQB 26 0 VQC 35 0 VQD 43 0 VSO 49 0
+ VNSO 80 0 VBQ 81 0 VST 88 0 VLCH 84 0 VNQB 87 0
.PLOT VCLK 2 0 VIN 55 0 VNCLK 56 0 VQ3 93 0 VQ2 92 0 VQ1 91 0 VQ0 90 0
+ VLCH 84 0
.PLOT VCLK 2 0 VLNBL 66 0 VLNOT 67 0 VPROG 68 0 VR3 58 0 VR2 60 0
+ VR1 62 0 VR0 64 0 VSCLK 94 0 VNSCLK 97 0 VDOFFQ 95 0
$ MACRO DEFINITION ////////////////////
.MACRO DFFFET 0 1 2 3 4 11 5 6
$ ------ NOR GATE AA
MAA1 7 4 0 ENHMD 10 0.6
DAA1 4 0 DIODE
MAA2 7 10 0 ENHMD 10 0.6
DAA2 10 0 DIODE
MAA3 7 8 0 ENHMD 10 0.6
DAA3 8 0 DIODE
MAAD 1 7 7 DEPMD 3 0.6
$ ------ NOR GATE A
MA1 8 7 0 ENHMD 10 0.6
DA1 7 0 DIODE
MA2 8 11 0 ENHMD 10 0.6
DA2 11 0 DIODE
MA3 8 2 0 ENHMD 10 0.6
DA3 2 0 DIODE
MAD 1 8 8 DEPMD 3 0.6
$ ------ NOR GATE B
MB1 9 8 0 ENHMD 10 0.6
DB1 8 0 DIODE
MB2 9 2 0 ENHMD 10 0.6
DB2 2 0 DIODE
MB3 9 10 0 ENHMD 10 0.6
DB3 10 0 DIODE
MBD 1 9 9 DEPMD 3 0.6
$ ------ NOR GATE BB
MBB1 10 9 0 ENHMD 10 0.6
DBB1 9 0 DIODE
MBB2 10 11 0 ENHMD 10 0.6
DBB2 11 0 DIODE
MBB3 10 3 0 ENHMD 10 0.6
DBB3 3 0 DIODE
MBBD 1 10 10 DEPMD 3 0.6
$ ------ NOR GATE Q
MQ1 5 4 0 ENHMD 10 0.6
DQ1 4 0 DIODE
MQ2 5 8 0 ENHMD 10 0.6
DQ2 8 0 DIODE
MQ3 5 6 0 ENHMD 10 0.6
DQ3 6 0 DIODE
MQD 1 5 5 DEPMD 3 0.6
$ ------ NOR GATE QB
MQB1 6 5 0 ENHMD 10 0.6
DQB1 5 0 DIODE
```

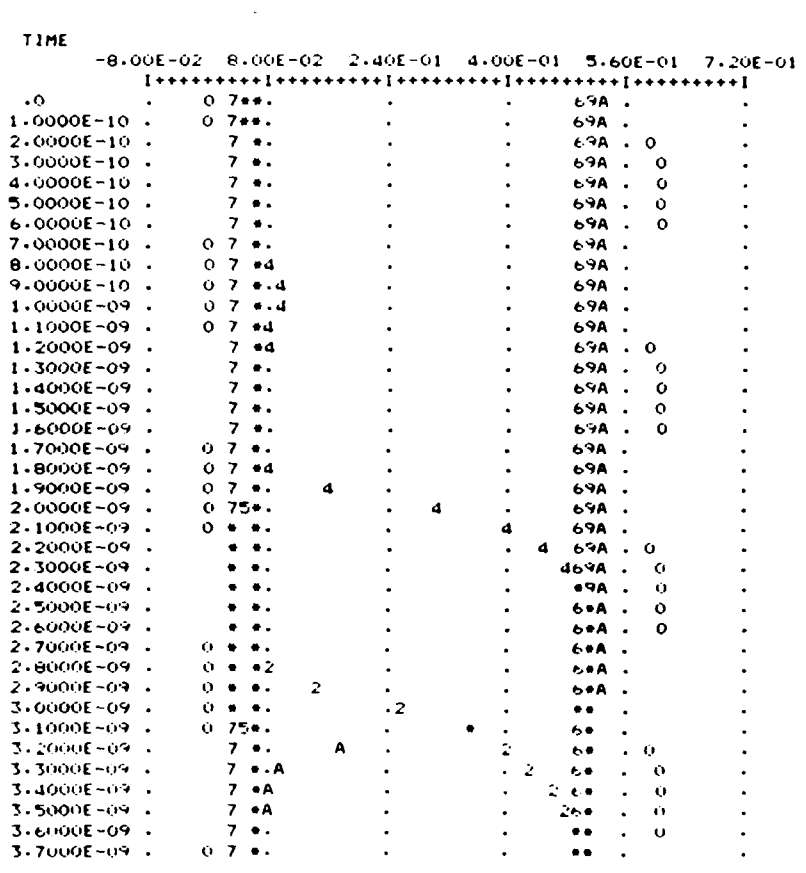
```
MQB2 6 9 0 ENHMD 10 0.6
DQB2 9 0 DIODE
MQB3 6 11 0 ENHMD 10 0.6
DQB3 11 0 DIODE
MQBD 1 6 6 DEPMD 3 0.6
.DCVOLT 5 0V 6 0.6V 7 0V 8 0.6V 9 0V 10 0V
.EOM
$ ======================================
.MACRO DLATCH 0 1 2 3 4 7
$ ------ NOR GATE A
MA1 5 2 0 ENHMD 10 0.6
DA1 2 0 DIODE
MA2 5 4 0 ENHMD 10 0.6
DA2 4 0 DIODE
MAD 1 5 5 DEPMD 3 0.6
$ ------ NOR GATE B
MB1 6 4 0 ENHMD 10 0.6
DB1 4 0 DIODE
MB2 6 3 0 ENHMD 10 0.6
DB2 3 0 DIODE
MBD 1 6 6 DEPMD 3 0.6
$ ------ NOR GATE Q
MQ1 7 5 0 ENHMD 10 0.6
DQ1 5 0 DIODE
MQ2 7 8 0 ENHMD 10 0.6
DQ2 8 0 DIODE
MQD 1 7 7 DEPMD 3 0.6
$ ------ NOR GATE QB
MQB1 8 7 0 ENHMD 10 0.6
DQB1 7 0 DIODE
MQB2 8 6 0 ENHMD 10 0.6
DQB2 6 0 DIODE
MQBD 1 8 8 DEPMD 3 0.6
.DCVOLT 7 0V 8 0.6V
.EOM
$ ======================================
.MACRO NOT 0 1 2 3
ME1 3 2 0 ENHMD 10 0.6
D1 2 0 DIODE
MD 1 3 3 DEPMD 3 0.6
.EOM
$ ======================================
.MACRO NOR2 0 1 2 3 4
ME1 4 2 0 ENHMD 10 0.6
D1 2 0 DIODE
ME2 4 3 0 ENHMD 10 0.6
D2 3 0 DIODE
MD 1 4 4 DEPMD 3 0.6
.EOM
$ ======================================
.MACRO NOR3 0 1 2 3 4 5
ME1 5 2 0 ENHMD 10 0.6
D1 2 0 DIODE
ME2 5 3 0 ENHMD 10 0.6
```

```
D2 3 0 DIODE
ME3 5 4 0 ENHMD 10 0.6
D3 4 0 DIODE
MD 1 5 5 DEPMD 3 0.6
.EOM
$ ======================================
.MACRO NOR4 0 1 2 3 4 5 6
ME1 6 2 0 ENHMD 10 0.6
D1 2 0 DIODE
ME2 6 3 0 ENHMD 10 0.6
D2 3 0 DIODE
ME3 6 4 0 ENHMD 10 0.6
D3 4 0 DIODE
ME4 6 5 0 ENHMD 10 0.6
D3 5 0 DIODE
MD 1 6 6 DEPMD 3 0.6
.EOM
$ ======================================
.MACRO BUFFER 0 1 2 6
$ STAGE A
MA1 3 2 0 ENHMD 20 0.6
DIA 2 0 DIODE 2
MA2 1 3 3 DEPMD 6 0.6
$ STAGE B
MB1 4 3 0 ENHMD 10 0.6
DIB 3 0 DIODE
MB2 1 4 4 DEPMD 3 0.6
$ STAGE C
MC1 5 3 0 ENHMD 20 0.6
DEC 3 0 DIODE 2
MC2 1 4 5 DEPMD 6 0.6
DDC 4 5 DIODE 0.6
$ STAGE D
MD1 6 5 0 ENHMD 70 0.6
DED 5 0 DIODE 7
MD2 1 3 6 DEPMD 30 0.6
DDD 3 6 DIODE 3
.EOM
$ ======================================
.MACRO NR5BFR 0 1 2 3 4 5 10 9
$ STAGE A
MAA 6 2 0 ENHMD 20 0.6
DAA 2 0 DIODE 2
MAB 6 3 0 ENHMD 20 0.6
DAB 3 0 DIODE 2
MAC 6 4 0 ENHMD 20 0.6
DAC 4 0 DIODE 2
MAD 6 5 0 ENHMD 20 0.6
DAD 5 0 DIODE 2
MAE 6 10 0 ENHMD 20 0.6
DAE 10 0 DIODE 2
MDA 1 6 6 DEPMD 6 0.6
$ STAGE B
MB1 7 6 0 ENHMD 10 0.6
```

```
DIB 6 0 DIODE
MB2 1 7 7 DEPMD 3 0.6
$ STAGE C
MC1 8 6 0 ENHMD 20 0.6
DEC 6 0 DIODE 2
MC2 1 7 8 DEPMD 6 0.6
DDC 7 8 DIODE 0.6
$ STAGE D
MD1 9 8 0 ENHMD 70 0.6
DED 8 0 DIODE 7
MD2 1 6 9 DEPMD 30 0.6
DDD 6 9 DIODE 3
.EOM
$ MACRO EXPANSIONS ////////////////////
$ === SEGMENT A ========================
XDFFA 0 1 2 11 57 0 12 13 DFFFET
XNGA1 0 1 12 14 NOT
XNGA2 0 1 12 15 NOT
XPSA1 0 1 13 16 NOT
XPSA2 0 1 13 17 NOT
XAS11 0 1 26 33 42 18 NOR3
XAS12 0 1 17 43 20 NOR2
XAS13 0 1 17 35 19 NOR2
XAS20 0 1 18 19 20 68 11 NOR4
$ === SEGMENT B ========================
XDFFB 0 1 2 21 57 0 22 23 DFFFET
XNGB1 0 1 22 24 NOT
XPSB1 0 1 23 25 NOT
XPSB2 0 1 23 26 NOT
XBS11 0 1 26 33 27 NOR2
XBS12 0 1 25 44 29 NOR2
XBS13 0 1 15 35 42 28 NOR3
XBS20 0 1 27 28 29 68 21 NOR4
$ === SEGMENT C ========================
XDFFC 0 1 2 30 57 0 31 32 DFFFET
XNGC1 0 1 31 33 NOT
XNGC2 0 1 31 33 NOT
XPSC1 0 1 32 34 NOT
XPSC2 0 1 32 35 NOT
XCS11 0 1 34 42 36 NOR2
XCS12 0 1 15 24 44 37 NOR3
XCS13 0 1 16 25 44 38 NOR3
XCS20 0 1 36 37 38 68 30 NOR4
$ === SEGMENT D ========================
XDFFD 0 1 2 39 57 0 40 41 DFFFET
XNGD1 0 1 40 42 NOT
XPSD1 0 1 41 43 NOT
XPSD2 0 1 41 44 NOT
XDS11 0 1 14 24 33 68 47 NOR4
XDS12 0 1 16 25 33 68 45 NOR4
XDS13 0 1 14 25 34 68 48 NOR4
XDS14 0 1 16 24 34 68 46 NOR4
XDS20 0 1 45 46 47 48 39 NOR4
$ === OUTPUT LOGIC =====================
```

```
XNOTB 0 1 26 87 NOT
XOFL1 0 1 17 87 35 43 49 NOR4
XINV1 0 1 49 80 NOT
XOFL2 0 1 80 81 83 NOR2
XOFL3 0 1 80 81 85 NOR2
XMBP0 0 1 80 82 81 NOR2
XMBN0 0 1 81 88 82 NOR2
XINV2 0 1 84 88 NOT
XLLCH 0 1 83 84 BUFFER
XHLCH 0 1 85 86 BUFFER
$ === SHIFT REGISTER ====================
XNCLK 0 1 2 56 BUFFER
$ --- SIMULATION OF ADDL LOAD ON BUFFER ---
MSRG1 75 56 0 ENHMD 120 7.2
DSRG1 56 0 DIODE 12
MSRG2 75 0 0 ENHMD 240 14.4
MSRGD 1 75 75 DEPMD 36 7.2
$ =======
XBLK3 0 1 56 55 57 0 58 59 DFFFET
XBLK2 0 1 56 58 57 0 60 61 DFFFET
XBLK1 0 1 56 60 57 0 62 63 DFFFET
XBLK0 0 1 56 62 57 0 64 65 DFFFET
$ === SYNC CIRCUITRY ====================
XLOGA 0 1 59 61 63 65 66 NOR4
XLGNA 0 1 66 67 NOT
XLOGB 0 1 0 0 0 67 95 68 NR5BFR
XSCLK 0 1 95 2 94 NOR2
XNSCL 0 1 94 97 NOT
XDOFF 0 1 97 68 57 0 95 96 DFFFET
$ === OUTPUT LATCHES ====================
XLCH3 0 1 58 59 84 93 DLATCH
XLCH2 0 1 60 61 84 92 DLATCH
XLCH1 0 1 62 63 84 91 DLATCH
XLCH0 0 1 64 65 84 90 DLATCH
$ --- SIMULATION OF 4 MORE LATCHES ---
MNORE1 73 84 0 ENHMD 80 4.8
DNOR1 84 0 DIODE 8
MNORE2 73 0 0 ENHMD 80 4.8
DNOR2 0 0 DIODE 8
MNORD 1 73 73 DEPMD 24 4.8
$ ///// MODEL PARAMETERS /////
.MODEL DEPMD NMOS BULK=0 VT=-0.5 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.MODEL ENHMD NMOS BULK=0 VT=0.15 UB=3500 TOX=300 DNB=1E17 VMX=2E7 CLM=1
.MODEL DIODE D IS=1E-14 CJA=10E-15 RS=100
$ ***********************************************************
VCLK 2 0 DC 0V PL 0V 100PS 0.6V 200PS 0.6V 600PS 0V 700PS
+ 0V 1100PS R 100PS
VRESET 57 0 DC 0V PL 0V 80PS 0.6V 180PS 0.6V 900PS 0V 1000PS
VQ4 55 0 DC 0V PL 0V 50PS 0.6V 150PS 0.6V 4.7NS 0V 4.8NS 0V 5.7NS
+ 0.6V 5.8NS 0.6V 6.7NS 0V 6.8NS 0V 7.7NS 0.6V 7.8NS 0.6V 8.7NS 0V 8.8NS
VCC 1 0 DC 2V
.END
```




TIME
-8.00E-02
8.00E-02
2.40E-01
4.00E-01
5.60E-01
7.20E-01

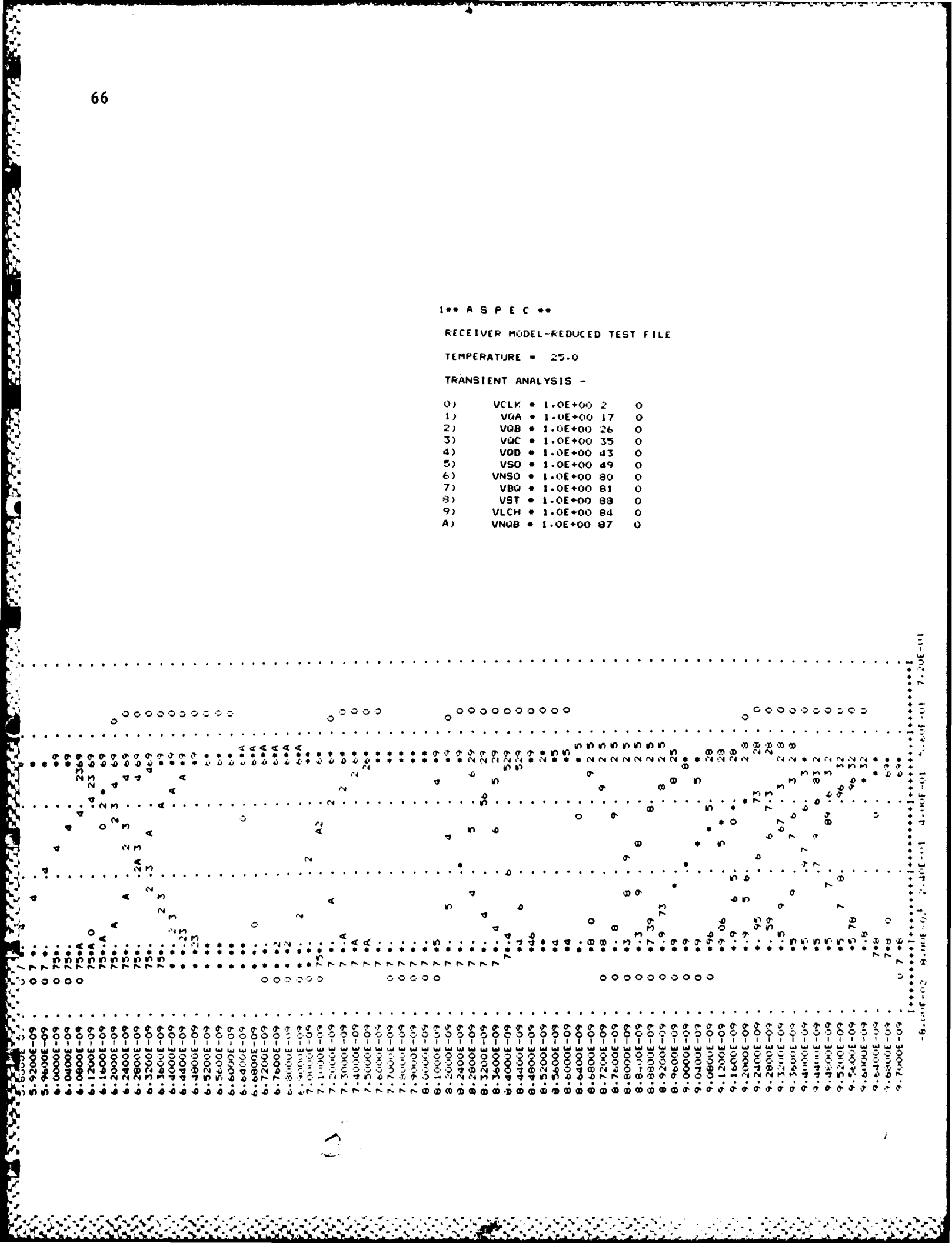
1** A S P E C **

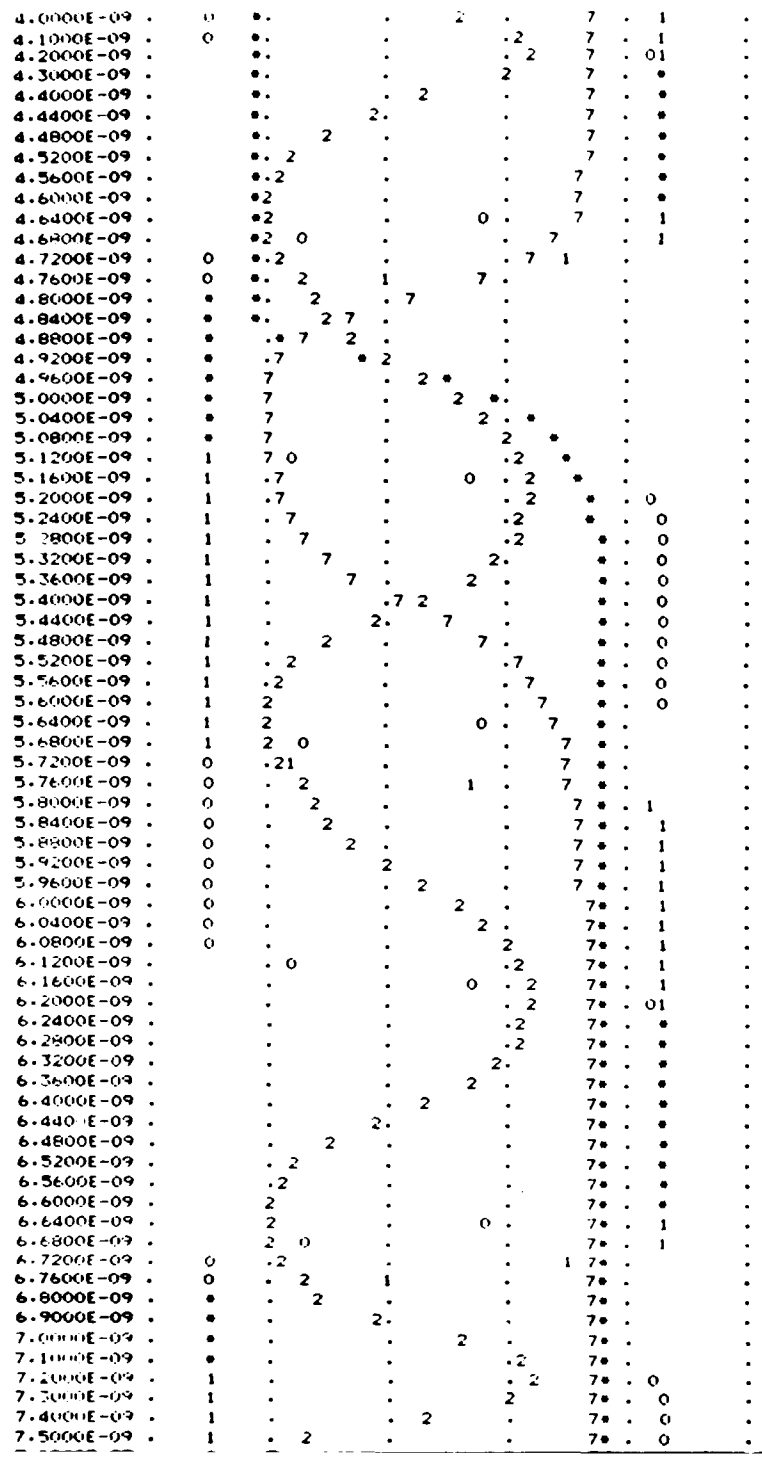
RECEIVER MODEL-REDUCED TEST FILE

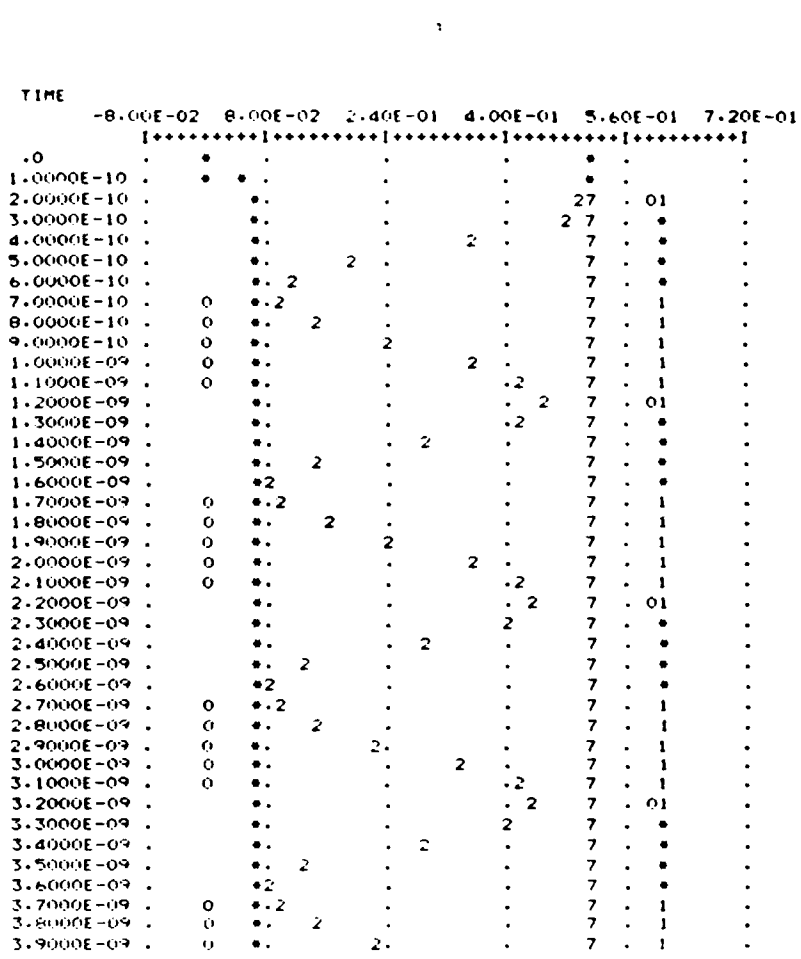
TEMPERATURE = 25.0

TRANSIENT ANALYSIS -

0)	VCLK	1.0E+00	2	0
1)	VQA	1.0E+00	17	0
2)	VQB	1.0E+00	26	0
3)	VQC	1.0E+00	35	0
4)	VQD	1.0E+00	43	0
5)	VSO	1.0E+00	49	0
6)	VNSO	1.0E+00	80	0
7)	VBQ	1.0E+00	81	0
8)	VST	1.0E+00	88	0
9)	VLCH	1.0E+00	84	0
A)	VNQB	1.0E+00	87	0






TIME
-8.00E-02
8.00E-02
2.40E-01
4.00E-01
5.60E-01
7.20E-01

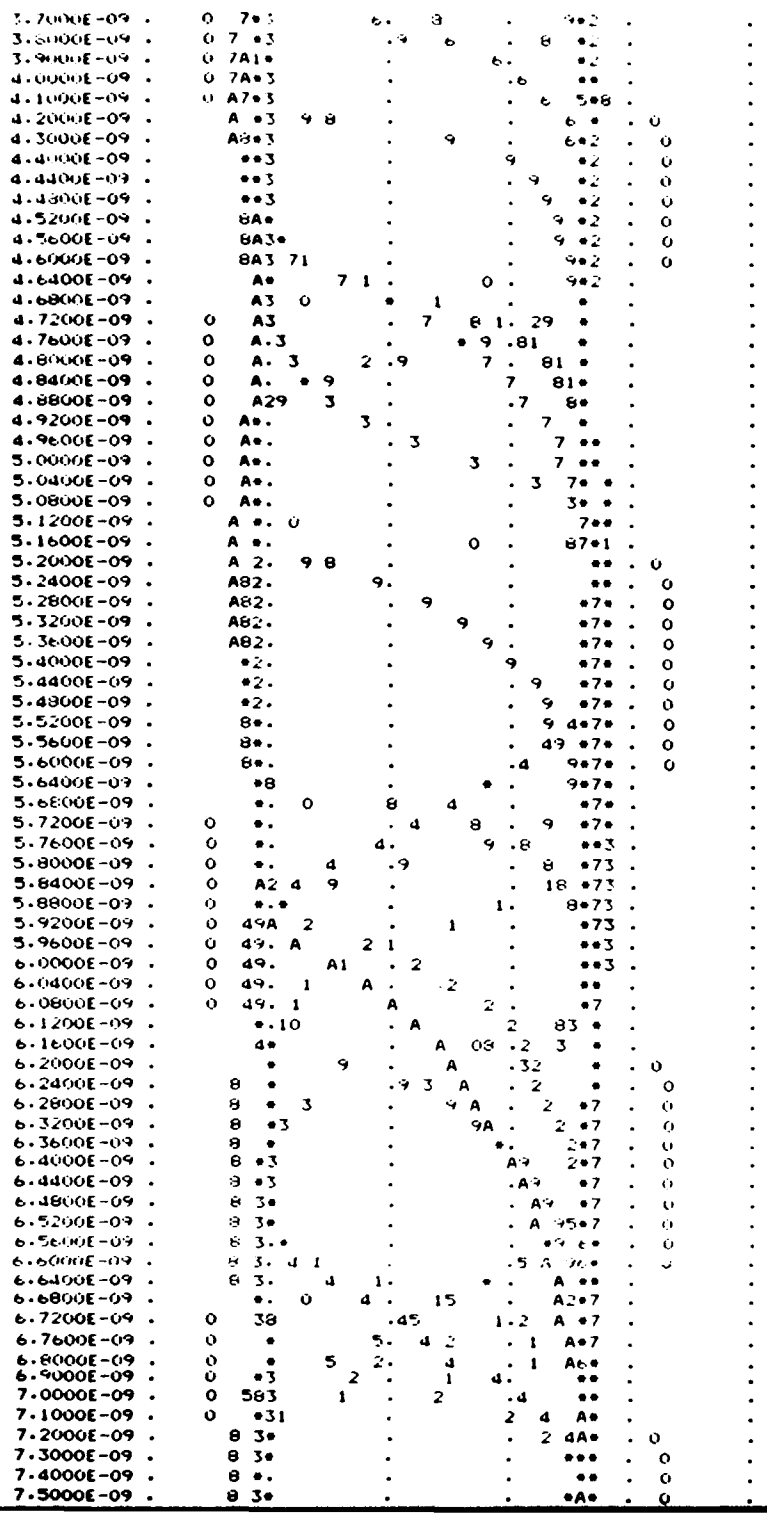
1** A S P E C **

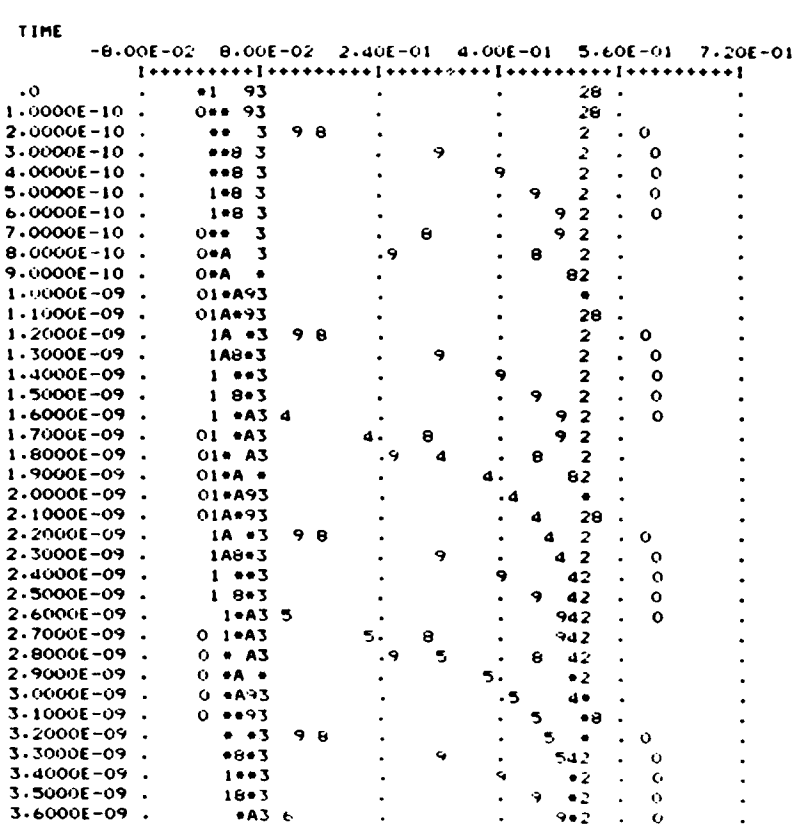
RECEIVER MODEL-REDUCED TEST FILE

TEMPERATURE = 25.0

TRANSIENT ANALYSIS -

0)	VCLK	* 1.0E+00	2	0
1)	VIN	* 1.0E+00	55	0
2)	VNCLK	* 1.0E+00	56	0
3)	VO3	* 1.0E+00	93	0
4)	VO2	* 1.0E+00	92	0
5)	VO1	* 1.0E+00	91	0
6)	VO0	* 1.0E+00	90	0
7)	VLCH	* 1.0E+00	84	0




TIME
-8.00E-02
8.00E-02
2.40E-01
4.00E-01
5.60E-01
7.20E-01

1** A S P E C **

RECEIVER MODEL-REDUCED TEST FILE

TEMPERATURE = 25.0

TRANSIENT ANALYSIS -

0)	VCLK	* 1.0E+00	2	0
1)	VLNBL	* 1.0E+00	66	0
2)	VLNOT	* 1.0E+00	67	0
3)	VPROG	* 1.0E+00	68	0
4)	VR3	* 1.0E+00	58	0
5)	VR2	* 1.0E+00	60	0
6)	VR1	* 1.0E+00	62	0
7)	VR0	* 1.0E+00	64	0
8)	VSCLK	* 1.0E+00	94	0
9)	VNSCLK	* 1.0E+00	97	0
A)	VDOFFQ	* 1.0E+00	95	0

```
COMPILE $
DIRECTORY: GOULD $
OPTIONS: REPL, NC=0 $
MODULE: TXMODL/GATE/1/GOULD $
INPUTS: CLOCK, RESET, RST, SET, SRLIN, I15, I14, I13, I12, I11, I10, I9, I8,
             I7, I6, I5, I4, I3, I2, I1, I0 $
OUTPUT: SRLOUT $
USE: DFET = DNORFF/GATE/1/GOULD,
     NOR3 = NOR(3,1),
     NOR4 = NOR(4,1),
     NOR2 = NOR(2,1) $
DEFINE:
   NCLK = NOT(CLOCK);
   "---STATE MACHINE IS 180 OUT OF PHASE WITH SHIFT REGISTER---"
   DFFA(Q-A, QB-A) = DFET(AS2, NCLK, RESET, SET );
   DFFB(Q-B, QB-B) = DFET(BS2, NCLK, RESET, SET );
   DFFC(Q-C, QB-C) = DFET(CS2, NCLK, RESET, SET );
   DFFD(Q-D, QB-D) = DFET(DS2, NCLK, RESET, SET );
   AS1-1 = NOR3(Q-B, QB-C, QB-D);
   AS1-2 = NOR2(Q-A, Q-D);
   AS1-3 = NOR2(Q-A, Q-C);
   AS2 = NOR3(AS1-1, AS1-2, AS1-3);
   BS1-1 = NOR2(Q-B, QB-C);
   BS1-2 = NOR2(Q-B, Q-D);
   BS1-3 = NOR3(QB-A, Q-C, QB-D);
   BS2 = NOR3(BS1-1, BS1-2, BS1-3);
   CS1-1 = NOR2(Q-C, QB-D);
   CS1-2 = NOR3(QB-A, QB-B, Q-D);
   CS1-3 = NOR3(Q-A, Q-B, Q-D);
   CS2 = NOR3(CS1-1, CS1-2, CS1-3);
   DS1-1 = NOR3(QB-A, QB-B, QB-C);
   DS1-2 = NOR3(Q-A, Q-B, QB-C);
   DS1-3 = NOR3(QB-A, Q-B, Q-C);
   DS1-4 = NOR3(Q-A, QB-B, Q-C);
   DS2 = NOR4(DS1-1, DS1-2, DS1-3, DS1-4);
   OFL1(SHIFT) = NOR4(Q-A, Q-B, Q-C, Q-D);
   INV1(LOAD) = NOT(OFL1);
   "---RESET OF SHIFT REGISTER IS GROUNDED---"
   B15-S = NOR2(SRLIN, SHIFT);
   B15-P = NOR2(I15, LOAD);
   B15 = NOR2(B15-S, B15-P);
   BLK15( Q15=Q ) = DFET(B15, CLOCK, RST, SET);
   B14-S = NOR2(Q15, SHIFT);
   B14-P = NOR2(I14, LOAD);
   B14 = NOR2(B14-S, B14-P);
   BLK14( Q14=Q ) = DFET(B14, CLOCK, RST, SET);
   B13-S = NOR2(Q14, SHIFT);
   B13-P = NOR2(I13, LOAD);
   B13 = NOR2(B13-S, B13-P);
   BLK13( Q13=Q ) = DFET(B13, CLOCK, RST, SET);
   B12-S = NOR2(Q13, SHIFT);
   B12-P = NOR2(I12, LOAD);
```

```
B12 = NOR2(B12-S, B12-P);
BLK12( Q12=Q ) = DFET(B12, CLOCK, RST, SET);
B11-S = NOR2(Q12, SHIFT);
B11-P = NOR2(I11, LOAD);
B11 = NOR2(B11-S, B11-P);
BLK11( Q11=Q ) = DFET(B11, CLOCK, RST, SET);
B10-S = NOR2(Q11, SHIFT);
B10-P = NOR2(I10, LOAD);
B10 = NOR2(B10-S, B10-P);
BLK10( Q10=Q ) = DFET(B10, CLOCK, RST, SET);
B9-S = NOR2(Q10, SHIFT);
B9-P = NOR2(I9, LOAD);
B9 = NOR2(B9-S, B9-P);
BLK9( Q9=Q ) = DFET(B9, CLOCK, RST, SET);
B8-S = NOR2(Q9, SHIFT);
B8-P = NOR2(I8, LOAD);
B8 = NOR2(B8-S, B8-P);
BLK8( Q8=Q ) = DFET(B8, CLOCK, RST, SET);
B7-S = NOR2(Q8, SHIFT);
B7-P = NOR2(I7, LOAD);
B7 = NOR2(B7-S, B7-P);
BLK7( Q7=Q ) = DFET(B7, CLOCK, RST, SET);
B6-S = NOR2(Q7, SHIFT);
B6-P = NOR2(I6, LOAD);
B6 = NOR2(B6-S, B6-P);
BLK6( Q6=Q ) = DFET(B6, CLOCK, RST, SET);
B5-S = NOR2(Q6, SHIFT);
B5-P = NOR2(I5, LOAD);
B5 = NOR2(B5-S, B5-P);
BLK5( Q5=Q ) = DFET(B5, CLOCK, RST, SET);
B4-S = NOR2(Q5, SHIFT);
B4-P = NOR2(I4, LOAD);
B4 = NOR2(B4-S, B4-P);
BLK4( Q4=Q ) = DFET(B4, CLOCK, RST, SET);
B3-S = NOR2(Q4, SHIFT);
B3-P = NOR2(I3, LOAD);
B3 = NOR2(B3-S, B3-P);
BLK3( Q3=Q ) = DFET(B3, CLOCK, RST, SET);
B2-S = NOR2(Q3, SHIFT);
B2-P = NOR2(I2, LOAD);
B2 = NOR2(B2-S, B2-P);
BLK2( Q2=Q ) = DFET(B2, CLOCK, RST, SET);
B1-S = NOR2(Q2, SHIFT);
B1-P = NOR2(I1, LOAD);
B1 = NOR2(B1-S, B1-P);
BLK1( Q1=Q ) = DFET(B1, CLOCK, RST, SET);
B0-S = NOR2(Q1, SHIFT);
B0-P = NOR2(I0, LOAD);
B0 = NOR2(B0-S, B0-P);
BLK0( SRLOUT= Q ) = DFET(B0, CLOCK, RST, SET);
```

```
END MODULE $
END COMPILE $
LOAD TXMODL/GATE/1/GOULD $
END TDL $
```

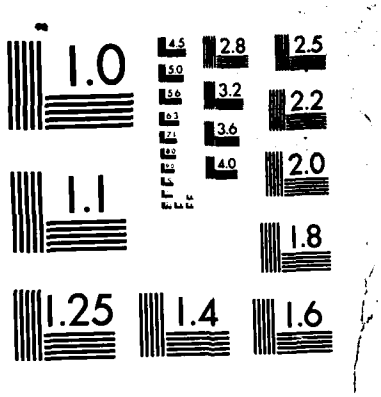
```
COMPILE $
DIRECTORY: GOULD $
OPTIONS: REPL, NC=0 $
MODULE: RXMODL/GATE/1/GOULD $
INPUTS: CLOCK, RESET, SET, SRLIN $
OUTPUTS: 015, 014, 013, 012, 011, 010, 09, 08, 07, 06, 05, 04, 03,
         02, 01, 00 $
USE: DFET = DNORFF/GATE/1/GOULD,
     DLCH = DLATCH/GATE/1/GOULD,
     NOR16 = NOR(16, 1),
     NOR3 = NOR(3,1),
     NOR4 = NOR(4,1),
     NOR2 = NOR(2,1) $
DEFINE:
   DFFA(Q-A, QB-A) = DFET(AS2, CLOCK, SYNCOFF, SET );
   DFFB(Q-B, QB-B) = DFET(BS2, CLOCK, SYNCOFF, SET );
   DFFC(Q-C, QB-C) = DFET(CS2, CLOCK, SYNCOFF, SET );
   DFFD(Q-D, QB-D) = DFET(DS2, CLOCK, SYNCOFF, SET );
   AS1-1 = NOR3(Q-B, QB-C, QB-D);
   AS1-2 = NOR2(Q-A, Q-D);
   AS1-3 = NOR2(Q-A, Q-C);
   AS2 = NOR3(AS1-1, AS1-2, AS1-3);
   BS1-1 = NOR2(Q-B, QB-C);
   BS1-2 = NOR2(Q-B, Q-D);
   BS1-3 = NOR3(QB-A, Q-C, QB-D);
   BS2 = NOR3(BS1-1, BS1-2, BS1-3);
   CS1-1 = NOR2(Q-C, QB-D);
   CS1-2 = NOR3(QB-A, QB-B, Q-D);
   CS1-3 = NOR3(Q-A, Q-B, Q-D);
   CS2 = NOR3(CS1-1, CS1-2, CS1-3);
   DS1-1 = NOR3(QB-A, QB-B, QB-C);
   DS1-2 = NOR3(Q-A, Q-B, QB-C);
   DS1-3 = NOR3(QB-A, Q-B, Q-C);
   DS1-4 = NOR3(Q-A, QB-B, Q C);
   DS2 = NOR4(DS1-1, DS1-2, DS1-3, DS1-4);
   OFL1 = NOR4(Q-A, Q-B, Q-C, Q-D);
   INV1 = NOT(OFL1);
   INV2 = NOT(CLOCK);
   OFL2 = NOR2(INV1, INV2);
   INV3(LATCH) = NOT(OFL2);
   NCLK = NOT(CLOCK);
   BLK15( Q15, QB15 ) = DFET(SRLIN, NCLK, RESET, SET);
   BLK14( Q14, QB14 ) = DFET(Q15, NCLK, RESET, SET);
   BLK13( Q13, QB13 ) = DFET(Q14, NCLK, RESET, SET);
   BLK12( Q12, QB12 ) = DFET(Q13, NCLK, RESET, SET);
   BLK11( Q11, QB11 ) = DFET(Q12, NCLK, RESET, SET);
   BLK10( Q10, QB10 ) = DFET(Q11, NCLK, RESET, SET);
   BLK9( Q9, QB9 ) = DFET(Q10, NCLK, RESET, SET);
   BLK8( Q8, QB8 ) = DFET(Q9, NCLK, RESET, SET);
   BLK7( Q7, QB7 ) = DFET(Q8, NCLK, RESET, SET);
   BLK6( Q6, QB6 ) = DFET(Q7, NCLK, RESET, SET);
   BLK5( Q5, QB5 ) = DFET(Q6, NCLK, RESET, SET);
```

```
    BLK4( Q4, QB4 ) = DFET(Q5, NCLK, RESET, SET);
    BLK3( Q3, QB3 ) = DFET(Q4, NCLK, RESET, SET);
    BLK2( Q2, QB2 ) = DFET(Q3, NCLK, RESET, SET);
    BLK1( Q1, QB1 ) = DFET(Q2, NCLK, RESET, SET);
    BLK0( Q0, QB0 ) = DFET(Q1, NCLK, RESET, SET);
    SYNCLOG = NOR16(QB15, QB14, QB13, QB12, QB11, QB10, QB9, QB8, QB7,
                    QB6, QB5, QB4, QB3, QB2, QB1, QB0);
    SFFQB = NOR2(RESET, SFFQ);
    SFFQ = NOR2(SYNCOFF, SFFQB);
    SNCLOGB = NOT(SYNCLOG);
    SYNCOFF = NOR2(SNCLOGB, SFFQB);
DLCH15( O15 ) = DLCH(Q15, QB15, LATCH);
DLCH14( O14 ) = DLCH(Q14, QB14, LATCH);
DLCH13( O13 ) = DLCH(Q13, QB13, LATCH);
DLCH12( O12 ) = DLCH(Q12, QB12, LATCH);
DLCH11( O11 ) = DLCH(Q11, QB11, LATCH);
DLCH10( O10 ) = DLCH(Q10, QB10, LATCH);
DLCH9( O9 ) = DLCH(Q9, QB9, LATCH);
DLCH8( O8 ) = DLCH(Q8, QB8, LATCH);
DLCH7( O7 ) = DLCH(Q7, QB7, LATCH);
DLCH6( O6 ) = DLCH(Q6, QB6, LATCH);
DLCH5( O5 ) = DLCH(Q5, QB5, LATCH);
DLCH4( O4 ) = DLCH(Q4, QB4, LATCH);
DLCH3( O3 ) = DLCH(Q3, QB3, LATCH);
DLCH2( O2 ) = DLCH(Q2, QB2, LATCH);
DLCH1( O1 ) = DLCH(Q1, QB1, LATCH);
DLCH0( O0 ) = DLCH(Q0, QB0, LATCH);
END MODULE $
END COMPILE $
LOAD RXMODL/GATE/1/GOULD $
END TDL$
```

```
1
 CC-TDL TEST GENERATION AND SIMULATION  VERSION  5, SIZE 1048K.
 FIRST QUARTER RELEASE
 COPYRIGHTED, 1983, BY CGIS/A COMSAT COMPANY
 DIGITAL DESIGN AND TEST DIVISION.  AUSTIN, TEXAS, USA.
 THIS CYBER VERSION WAS UPDATED 04/11/84 AT 11.12.09

   10/03/85  16.10.53


 TCC     1.  MODE 2 $
 TCC     2.  LOAD $

 LOADED MODULE  TXMODL



 TCC     3.  SAVE SIGNALS CLOCK, DL4CLK, RESET, Q-A, Q-B, Q-C, Q-D, LOAD, SHIFT,
 TCC     4.       SRLOUT $
 TCC     5.  SIMSETUP $

 AS SIMSETUP STARTS PROCESSING, 1043269 WORDS OF FREE SPACE IS AVAILABLE.

 TSS     6.  STOPSIM 200 $
 END OF SIMULATION SCHEDULED FOR TIME       200.
 TSS     7.  CHANGE CLOCK 1 0, 200, 10 $
 TSS     8.  CHANGE CLOCK 0 5, 200, 10 $
 TSS     9.  CHANGE RESET 1 0 $
 TSS    10.  CHANGE RESET 0 8 $
 TSS    11.  CHANGE SET 0 0 $
 TSS    12.  CHANGE SRLIN 0 0 $
 TSS    13.  CHANGE I15, I14, I 2, I11, I9, I8, I7, I6, I4, I3, I1, I0 1 0 $
 TSS    14.  CHANGE I13, I10, .5, I2 0 0 $
 TSS    15.  END SETUP $

 AT THE END OF SIMSETUP, THERE ARE  1042959 WORDS OF FREE SPACE LEFT.

 TCC    16.  SIMULATE 200 $
 END OF SIMULATION SCHEDULED FOR TIME       200.

 MODE 2 SIMULATION COMMENCED.
 NET IS FIRST INITIALIZED AT TIME        23
 SIMULATION STOPPED AT TIME       200 FOR THE FOLLOWING REASON.
     A SCHEDULED STOP
 TCC    17.  DISPLAY SIGNALS CLOCK, DL4CLK, RESET, Q-A, Q-B, Q-C, Q-D, LOAD, SHIF

T,
 TCC    18.          SRLOUT $
```

AD-A166 060 A GAAS BASED DIGITAL SERIAL COMMUNICATIONS SYSTEM(U) 2/2
ARMY MILITARY PERSONNEL CENTER ALEXANDRIA VA
R Z ROSARIO 25 MAR 86

UNCLASSIFIED F/G 17/2 NL



1

PAGE 1. 1

TIME	(CLOCK)	25	(RESET)	Q-A	Q-B	Q-C	Q-D	LOAD	SHIFT	(SRLOUT)
0	1	XXX	1	XXX	XXX	XXX	XXX	XXX	XXX	XXX
1	1	XXX	1	0	0	0	0	XXX	XXX	XXX
2	1	XXX	1	0	0	0	0	XXX	XXX	0
4	1	1	1	0	0	0	0	XXX	XXX	0
5	0	1	1	0	0	0	0	XXX	XXX	0
6	0	1	1	0	0	0	0	0	XXX	0
8	0	1	0	0	0	0	0	0	XXX	0
9	0	0	0	0	0	0	0	0	XXX	0
10	1	0	0	0	0	0	0	0	1	0
13	1	0	0	0	0	0	0	0	1	XXX
14	1	1	0	0	0	0	0	0	1	XXX
15	0	1	0	0	0	0	0	0	1	XXX
18	0	1	0	0	0	0	1	0	1	XXX
19	0	0	0	0	0	0	1	0	1	XXX
20	1	0	0	0	0	0	1	0	1	XXX
23	1	0	0	0	0	0	1	1	1	1
24	1	1	0	0	0	0	1	1	1	1
25	0	1	0	0	0	0	1	1	1	1
27	0	1	0	0	0	0	1	1	0	1
28	0	1	0	0	1	0	1	1	0	1
29	0	0	0	0	1	0	1	1	0	1
30	1	0	0	0	1	0	1	1	0	1
34	1	1	0	0	1	0	1	1	0	1
35	0	1	0	0	1	0	1	1	0	1
37	0	1	0	0	1	0	0	1	0	1
39	0	0	0	0	1	0	0	1	0	1
40	1	0	0	0	1	0	0	1	0	1
42	1	0	0	0	1	0	0	1	0	0
44	1	1	0	0	1	0	0	1	0	0
45	0	1	0	0	1	0	0	1	0	0
46	0	1	0	0	1	0	0	1	0	0
48	0	1	0	0	1	1	0	1	0	0
49	0	0	0	0	1	1	0	1	0	0
50	1	0	0	0	1	1	0	1	0	0
53	1	0	0	0	1	1	0	1	0	1
54	1	1	0	0	1	1	0	1	0	1
55	0	1	0	0	1	1	0	1	0	1
58	0	1	0	0	1	1	1	1	0	1
59	0	0	0	0	1	1	1	1	0	1
60	1	0	0	0	1	1	1	1	0	1
64	1	1	0	0	1	1	1	1	0	1
65	0	1	0	0	1	1	1	1	0	1
68	0	1	0	1	1	1	1	1	0	1

1

TIME	(CLOCK)	25	(RESET)	Q-A	Q-B	Q-C	Q-D	LOAD	SHIFT	(SRLOUT)
69	0	0	0	1	1	1	1	1	0	1
70	1	0	0	1	1	1	1	1	0	1
72	1	0	0	1	1	1	1	1	0	0
74	1	1	0	1	1	1	1	1	0	0
75	0	1	0	1	1	1	1	1	0	0
77	0	1	0	1	1	1	0	1	0	0
79	0	0	0	1	1	1	0	1	0	0
80	1	0	0	1	1	1	0	1	0	0
83	1	0	0	1	1	1	0	1	0	1
84	1	1	0	1	1	1	0	1	0	1
85	0	1	0	1	1	1	0	1	0	1
87	0	1	0	1	1	0	0	1	0	1
89	0	0	0	1	1	0	0	1	0	1
90	1	0	0	1	1	0	0	1	0	1
94	1	1	0	1	1	0	0	1	0	1
95	0	1	0	1	1	0	0	1	0	1
98	0	1	0	1	1	0	1	1	0	1
99	0	0	0	1	1	0	1	1	0	1
100	1	0	0	1	1	0	1	1	0	1
104	1	1	0	1	1	0	1	1	0	1
105	0	1	0	1	1	0	1	1	0	1
107	0	1	0	1	0	0	1	1	0	1
109	0	0	0	1	0	0	1	1	0	1
110	1	0	0	1	0	0	1	1	0	1
114	1	1	0	1	0	0	1	1	0	1
115	0	1	0	1	0	0	1	1	0	1
117	0	1	0	1	0	0	0	1	0	1
119	0	0	0	1	0	0	0	1	0	1
120	1	0	0	1	0	0	0	1	0	1
122	1	0	0	1	0	0	0	1	0	0
124	1	1	0	1	0	0	0	1	0	0
125	0	1	0	1	0	0	0	1	0	0
128	0	1	0	1	0	1	0	1	0	0
129	0	0	0	1	0	1	0	1	0	0
130	1	0	0	1	0	1	0	1	0	0
133	1	0	0	1	0	1	0	1	0	1
134	1	1	0	1	0	1	0	1	0	1
135	0	1	0	1	0	1	0	1	0	1
138	0	1	0	1	0	1	1	1	0	1
139	0	0	0	1	0	1	1	1	0	1
140	1	0	0	1	0	1	1	1	0	1
144	1	1	0	1	0	1	1	1	0	1
145	0	1	0	1	0	1	1	1	0	1

1 PAGE 1. 3

TIME	(CLOCK)	25	(RESET)	Q-A	Q-B	Q-C	Q-D	LOAD	SHIFT	(SRLOUT)
147	0	1	0	0	0	1	1	1	0	1
149	0	0	0	0	0	1	1	1	0	1
150	1	0	0	0	0	1	1	1	0	1
152	1	0	0	0	0	1	1	1	0	0
154	1	1	0	0	0	1	1	1	0	0
155	0	1	0	0	0	1	1	1	0	0
157	0	1	0	0	0	1	0	1	0	0
159	0	0	0	0	0	1	0	1	0	0
160	1	0	0	0	0	1	0	1	0	0
163	1	0	0	0	0	1	0	1	0	1
164	1	1	0	0	0	1	0	1	0	1
165	0	1	0	0	0	1	0	1	0	1
167	0	1	0	0	0	0	0	1	0	1
169	0	0	0	0	0	0	0	1	0	1
170	1	0	0	0	0	0	0	1	0	1
172	1	0	0	0	0	0	0	0	0	1
174	1	1	0	0	0	0	0	0	0	1
175	0	1	0	0	0	0	0	0	0	1
176	0	1	0	0	0	0	0	0	1	1
178	0	1	0	0	0	0	1	0	1	1
179	0	0	0	0	0	0	1	0	1	1
180	1	0	0	0	0	0	1	0	1	1
182	1	0	0	0	0	0	1	0	1	0
183	1	0	0	0	0	0	1	1	1	0
184	1	1	0	0	0	0	1	1	1	0
185	0	1	0	0	0	0	1	1	1	0
187	0	1	0	0	0	0	1	1	0	0
188	0	1	0	0	1	0	1	1	0	0
189	0	0	0	0	1	0	1	1	0	0
190	1	0	0	0	1	0	1	1	0	0
194	1	1	0	0	1	0	1	1	0	0
195	0	1	0	0	1	0	1	1	0	0
197	0	1	0	0	1	0	0	1	0	0
199	0	0	0	0	1	0	0	1	0	0
200	1	0	0	0	1	0	0	1	0	0

1

TCC 19. END $

*** 184 SIGNAL VALUE RECORDS ARE WRITTEN TO THE SAVE FILE

```
1
 CC-TDL TEST GENERATION AND SIMULATION  VERSION  5, SIZE 1048K.
 FIRST QUARTER RELEASE
 COPYRIGHTED, 1983, BY CGIS/A COMSAT COMPANY
 DIGITAL DESIGN AND TEST DIVISION.  AUSTIN, TEXAS, USA.
 THIS CYBER VERSION WAS UPDATED 04/11/84 AT 11.12.09

   10/03/85  14.44.02


 TCC     1.  MODE 2 $
 TCC     2.  LOAD $

 LOADED MODULE  RXMODL



 TCC     3.  SAVE SIGNALS CLOCK, DL1NCLK, RESET, SRLIN, SPRSCLK, NSPRSCL, DL1QOFF

,
 TCC     4.  DL3SYNCLOG, DL3LATCH, 015, 014, 013, 012, 011, 010, 09, 08, 07, 06,
 TCC     5.  05, 04, 03, 02, 01, 00 $
 TCC     6.  SIMSETUP $

 AS SIMSETUP STARTS PROCESSING, 1042608 WORDS OF FREE SPACE IS AVAILABLE.

 TSS     7.  STOPSIM 660 $
 END OF SIMULATION SCHEDULED FOR TIME       660.
 TSS     8.  CHANGE CLOCK 1 0, 660, 10 $
 TSS     9.  CHANGE CLOCK 0 5, 660, 10 $
 TSS    10.  CHANGE RESET 1 0 $
 TSS    11.  CHANGE RESET 0 8 $
 TSS    12.  CHANGE SET 0 0 $
 TSS    13.  CHANGE SRLIN 0 0 $
 TSS    14.  CHANGE SRLIN 1 7 $
 TSS    15.  CHANGE SRLIN 0 167 $
 TSS    16.  CHANGE SRLIN 1 327 $
 TSS    17.  CHANGE SRLIN 0 347 $
 TSS    18.  CHANGE SRLIN 1 357 $
 TSS    19.  CHANGE SRLIN 0 377 $
 TSS    20.  CHANGE SRLIN 1 387 $
 TSS    21.  CHANGE SRLIN 0 427 $
 TSS    22.  CHANGE SRLIN 1 437 $
 TSS    23.  CHANGE SRLIN 0 457 $
 TSS    24.  CHANGE SRLIN 1 467 $
 TSS    25.  CHANGE SRLIN 0 507 $
 TSS    26.  END SETUP $
```

```
 AT THE END OF SIMSETUP, THERE ARE  1041766 WORDS OF FREE SPACE LEFT.

 TCC    27.  SIMULATE 660 $
 END OF SIMULATION SCHEDULED FOR TIME       660.

 MODE 2 SIMULATION COMMENCED.
 NET IS FIRST INITIALIZED AT TIME       169
 SIMULATION STOPPED AT TIME       660 FOR THE FOLLOWING REASON.
     A SCHEDULED STOP
 TCC    28.  DISPLAY SIGNALS CLOCK, DL1NCLK, RESET, SRLIN, SPRSCLK, NSPRSCL, DL1Q

OFF,
 TCC    29.  DL3SYNCLOG, DL3LATCH, O15, O14, O13, O12, O11, O10, O9, O8, O7, O6,
 TCC    30.  O5, O4, O3, O2, O1, O0 $
```

TIME	(CLOCK)	75	(RESET)	(SRLIN)	184	185	192	183	70	(0115)	(0114)
0	1	XXX	1	0	XXX	XXX	XXX	XXX	XXX	XXX	XXX
1	1	XXX	1	0	0	XXX	XXX	XXX	XXX	XXX	XXX
2	1	0	1	0	0	1	0	XXX	XXX	XXX	XXX
5	0	0	1	0	0	1	0	XXX	XXX	XXX	XXX
6	0	0	1	0	1	1	0	XXX	XXX	XXX	XXX
7	0	1	1	1	1	0	0	XXX	XXX	XXX	XXX
8	0	1	0	1	1	0	0	XXX	XXX	XXX	XXX
10	1	1	0	1	1	0	0	XXX	XXX	XXX	XXX
11	1	1	0	1	0	0	0	0	1	XXX	XXX
12	1	0	0	1	0	1	0	0	1	XXX	XXX
15	0	0	0	1	0	1	0	0	1	XXX	XXX
16	0	0	0	1	1	1	0	0	1	XXX	XXX
17	0	1	0	1	1	0	0	0	1	XXX	XXX
20	1	1	0	1	1	0	0	0	1	XXX	XXX
21	1	1	0	1	0	0	0	0	1	XXX	XXX
22	1	0	0	1	0	1	0	0	1	XXX	XXX
25	0	0	0	1	0	1	0	0	1	XXX	XXX
26	0	0	0	1	1	1	0	0	1	XXX	XXX
27	0	1	0	1	1	0	0	0	1	XXX	XXX
30	1	1	0	1	1	0	0	0	1	XXX	XXX
31	1	1	0	1	0	0	0	0	1	XXX	XXX
32	1	0	0	1	0	1	0	0	1	XXX	XXX
35	0	0	0	1	0	1	0	0	1	XXX	XXX
36	0	0	0	1	1	1	0	0	1	XXX	XXX
37	0	1	0	1	1	0	0	0	1	XXX	XXX
40	1	1	0	1	1	0	0	0	1	XXX	XXX
41	1	1	0	1	0	0	0	0	1	XXX	XXX
42	1	0	0	1	0	1	0	0	1	XXX	XXX
45	0	0	0	1	0	1	0	0	1	XXX	XXX
46	0	0	0	1	1	1	0	0	1	XXX	XXX
47	0	1	0	1	1	0	0	0	1	XXX	XXX
50	1	1	0	1	1	0	0	0	1	XXX	XXX
51	1	1	0	1	0	0	0	0	1	XXX	XXX
52	1	0	0	1	0	1	0	0	1	XXX	XXX
55	0	0	0	1	0	1	0	0	1	XXX	XXX
56	0	0	0	1	1	1	0	0	1	XXX	XXX
57	0	1	0	1	1	0	0	0	1	XXX	XXX
60	1	1	0	1	1	0	0	0	1	XXX	XXX
61	1	1	0	1	0	0	0	0	1	XXX	XXX
62	1	0	0	1	0	1	0	0	1	XXX	XXX
65	0	0	0	1	0	1	0	0	1	XXX	XXX
66	0	0	0	1	1	1	0	0	1	XXX	XXX
67	0	1	0	1	1	0	0	0	1	XXX	XXX

TIME	(CLOCK)	75	(RESET)	(SRLIN)	184	185	192	183	70	(0155)	(0144)
70	1	1	0	1	1	0	0	0	1	XXX	XXX
71	1	1	0	1	0	0	0	0	1	XXX	XXX
72	1	0	0	1	0	1	0	0	1	XXX	XXX
75	0	0	0	1	0	1	0	0	1	XXX	XXX
76	0	0	0	1	1	1	0	0	1	XXX	XXX
77	0	1	0	1	1	0	0	0	1	XXX	XXX
80	1	1	0	1	1	0	0	0	1	XXX	XXX
81	1	1	0	1	0	0	0	0	1	XXX	XXX
82	1	0	0	1	0	1	0	0	1	XXX	XXX
85	0	0	0	1	0	1	0	0	1	XXX	XXX
86	0	0	0	1	1	1	0	0	1	XXX	XXX
87	0	1	0	1	1	0	0	0	1	XXX	XXX
90	1	1	0	1	1	0	0	0	1	XXX	XXX
91	1	1	0	1	0	0	0	0	1	XXX	XXX
92	1	0	0	1	0	1	0	0	1	XXX	XXX
95	0	0	0	1	0	1	0	0	1	XXX	XXX
96	0	0	0	1	1	1	0	0	1	XXX	XXX
97	0	1	0	1	1	0	0	0	1	XXX	XXX
100	1	1	0	1	1	0	0	0	1	XXX	XXX
101	1	1	0	1	0	0	0	0	1	XXX	XXX
102	1	0	0	1	0	1	0	0	1	XXX	XXX
105	0	0	0	1	0	1	0	0	1	XXX	XXX
106	0	0	0	1	1	1	0	0	1	XXX	XXX
107	0	1	0	1	1	0	0	0	1	XXX	XXX
110	1	1	0	1	1	0	0	0	1	XXX	XXX
111	1	1	0	1	0	0	0	0	1	XXX	XXX
112	1	0	0	1	0	1	0	0	1	XXX	XXX
115	0	0	0	1	0	1	0	0	1	XXX	XXX
116	0	0	0	1	1	1	0	0	1	XXX	XXX
117	0	1	0	1	1	0	0	0	1	XXX	XXX
120	1	1	0	1	1	0	0	0	1	XXX	XXX
121	1	1	0	1	0	0	0	0	1	XXX	XXX
122	1	0	0	1	0	1	0	0	1	XXX	XXX
125	0	0	0	1	0	1	0	0	1	XXX	XXX
126	0	0	0	1	1	1	0	0	1	XXX	XXX
127	0	1	0	1	1	0	0	0	1	XXX	XXX
130	1	1	0	1	1	0	0	0	1	XXX	XXX
131	1	1	0	1	0	0	0	0	1	XXX	XXX
132	1	0	0	1	0	1	0	0	1	XXX	XXX
135	0	0	0	1	0	1	0	0	1	XXX	XXX
136	0	0	0	1	1	1	0	0	1	XXX	XXX
137	0	1	0	1	1	0	0	0	1	XXX	XXX
140	1	1	0	1	1	0	0	0	1	XXX	XXX

TIME	(CLOCK)	75	(RESET)	(SRLIN)	184	185	192	183	70	(015)	(014)
141	1	1	0	1	0	0	0	0	1	XXX	XXX
142	1	0	0	1	0	1	0	0	1	XXX	XXX
145	0	0	0	1	0	1	0	0	1	XXX	XXX
146	0	0	0	1	1	1	0	0	1	XXX	XXX
147	0	1	0	1	1	0	0	0	1	XXX	XXX
150	1	1	0	1	1	0	0	0	1	XXX	XXX
151	1	1	0	1	0	0	0	0	1	XXX	XXX
152	1	0	0	1	0	1	0	0	1	XXX	XXX
155	0	0	0	1	0	1	0	0	1	XXX	XXX
156	0	0	0	1	1	1	0	0	1	XXX	XXX
157	0	1	0	1	1	0	0	0	1	XXX	XXX
160	1	1	0	1	1	0	0	0	1	XXX	XXX
161	1	1	0	1	0	0	0	0	1	XXX	XXX
162	1	0	0	1	0	1	0	0	1	XXX	XXX
165	0	0	0	1	0	1	0	0	1	XXX	XXX
166	0	0	0	1	1	1	0	0	0	XXX	XXX
167	0	1	0	0	1	0	0	0	0	XXX	XXX
169	0	1	0	0	1	0	0	0	0	1	1
170	1	1	0	0	1	0	0	1	0	1	1
171	1	1	0	0	0	0	0	1	0	1	1
172	1	0	0	0	0	1	0	1	0	1	1
174	1	0	0	0	0	1	0	1	1	1	1
175	0	0	0	0	0	1	0	1	1	1	1
176	0	0	0	0	1	1	0	1	1	1	1
177	0	1	0	0	1	0	0	1	1	1	1
180	1	1	0	0	1	0	0	1	1	1	1
181	1	1	0	0	0	0	1	0	1	1	1
182	1	0	0	0	0	1	1	0	1	1	1
185	0	0	0	0	0	1	1	0	1	1	1
187	0	1	0	0	0	1	1	0	1	1	1
190	1	1	0	0	0	1	1	0	1	1	1
192	1	0	0	0	0	1	1	0	1	1	1
195	0	0	0	0	0	1	1	0	1	1	1
197	0	1	0	0	0	1	1	0	1	1	1
200	1	1	0	0	0	1	1	0	1	1	1
202	1	0	0	0	0	1	1	0	1	1	1
205	0	0	0	0	0	1	1	0	1	1	1
207	0	1	0	0	0	1	1	0	1	1	1
210	1	1	0	0	0	1	1	0	1	1	1
212	1	0	0	0	0	1	1	0	1	1	1
215	0	0	0	0	0	1	1	0	1	1	1
217	0	1	0	0	0	1	1	0	1	1	1
220	1	1	0	0	0	1	1	0	1	1	1

TIME	(CLOCK)	75	(RESET)	(SRLIN)	184	185	192	183	70	(0150)	(0140)
222	1	0	0	0	0	1	1	0	1	1	1
225	0	0	0	0	0	1	1	0	1	1	1
227	0	1	0	0	0	1	1	0	1	1	1
230	1	1	0	0	0	1	1	0	1	1	1
232	1	0	0	0	0	1	1	0	1	1	1
235	0	0	0	0	0	1	1	0	1	1	1
237	0	1	0	0	0	1	1	0	1	1	1
240	1	1	0	0	0	1	1	0	1	1	1
242	1	0	0	0	0	1	1	0	1	1	1
245	0	0	0	0	0	1	1	0	1	1	1
247	0	1	0	0	0	1	1	0	1	1	1
250	1	1	0	0	0	1	1	0	1	1	1
252	1	0	0	0	0	1	1	0	1	1	1
255	0	0	0	0	0	1	1	0	1	1	1
257	0	1	0	0	0	1	1	0	1	1	1
260	1	1	0	0	0	1	1	0	1	1	1
262	1	0	0	0	0	1	1	0	1	1	1
265	0	0	0	0	0	1	1	0	1	1	1
267	0	1	0	0	0	1	1	0	1	1	1
270	1	1	0	0	0	1	1	0	1	1	1
272	1	0	0	0	0	1	1	0	1	1	1
275	0	0	0	0	0	1	1	0	1	1	1
277	0	1	0	0	0	1	1	0	1	1	1
280	1	1	0	0	0	1	1	0	1	1	1
282	1	0	0	0	0	1	1	0	1	1	1
285	0	0	0	0	0	1	1	0	1	1	1
287	0	1	0	0	0	1	1	0	1	1	1
290	1	1	0	0	0	1	1	0	1	1	1
292	1	0	0	0	0	1	1	0	1	1	1
295	0	0	0	0	0	1	1	0	1	1	1
297	0	1	0	0	0	1	1	0	1	1	1
300	1	1	0	0	0	1	1	0	1	1	1
302	1	0	0	0	0	1	1	0	1	1	1
305	0	0	0	0	0	1	1	0	1	1	1
307	0	1	0	0	0	1	1	0	1	1	1
310	1	1	0	0	0	1	1	0	1	1	1
312	1	0	0	0	0	1	1	0	1	1	1
315	0	0	0	0	0	1	1	0	1	1	1
317	0	1	0	0	0	1	1	0	1	1	1
320	1	1	0	0	0	1	1	0	1	1	1
322	1	0	0	0	0	1	1	0	1	1	1
325	0	0	0	0	0	1	1	0	1	1	1
326	0	0	0	0	0	1	1	0	0	1	1

TIME	(CLOCK)	75	(RESET)	(SRLIN)	184	185	192	183	70	(015)	(014)
327	0	1	0	1	0	1	1	0	0	1	1
328	0	1	0	1	0	1	1	0	0	0	0
330	1	1	0	1	0	1	1	0	0	0	0
332	1	0	0	1	0	1	1	0	0	0	0
334	1	0	0	1	0	1	1	0	1	0	0
335	0	0	0	1	0	1	1	0	1	0	0
337	0	1	0	1	0	1	1	0	1	0	0
340	1	1	0	1	0	1	1	0	1	0	0
342	1	0	0	1	0	1	1	0	1	0	0
345	0	0	0	1	0	1	1	0	1	0	0
347	0	1	0	0	0	1	1	0	1	0	0
350	1	1	0	0	0	1	1	0	1	0	0
352	1	0	0	0	0	1	1	0	1	0	0
355	0	0	0	0	0	1	1	0	1	0	0
357	0	1	0	1	0	1	1	0	1	0	0
360	1	1	0	1	0	1	1	0	1	0	0
362	1	0	0	1	0	1	1	0	1	0	0
365	0	0	0	1	0	1	1	0	1	0	0
367	0	1	0	1	0	1	1	0	1	0	0
370	1	1	0	1	0	1	1	0	1	0	0
372	1	0	0	1	0	1	1	0	1	0	0
375	0	0	0	1	0	1	1	0	1	0	0
377	0	1	0	0	0	1	1	0	1	0	0
380	1	1	0	0	0	1	1	0	1	0	0
382	1	0	0	0	0	1	1	0	1	0	0
385	0	0	0	0	0	1	1	0	1	0	0
387	0	1	0	1	0	1	1	0	1	0	0
390	1	1	0	1	0	1	1	0	1	0	0
392	1	0	0	1	0	1	1	0	1	0	0
395	0	0	0	1	0	1	1	0	1	0	0
397	0	1	0	1	0	1	1	0	1	0	0
400	1	1	0	1	0	1	1	0	1	0	0
402	1	0	0	1	0	1	1	0	1	0	0
405	0	0	0	1	0	1	1	0	1	0	0
407	0	1	0	1	0	1	1	0	1	0	0
410	1	1	0	1	0	1	1	0	1	0	0
412	1	0	0	1	0	1	1	0	1	0	0
415	0	0	0	1	0	1	1	0	1	0	0
417	0	1	0	1	0	1	1	0	1	0	0
420	1	1	0	1	0	1	1	0	1	0	0
422	1	0	0	1	0	1	1	0	1	0	0
425	0	0	0	1	0	1	1	0	1	0	0
427	0	1	0	0	0	1	1	0	1	0	0

TIME	(CLOCK)	75	(RESET)	(SRLIN)	184	185	192	183	70	(015)	(014)
430	1	1	0	0	0	1	1	0	1	0	0
432	1	0	0	0	0	1	1	0	1	0	0
435	0	0	0	0	0	1	1	0	1	0	0
437	0	1	0	1	0	1	1	0	1	0	0
440	1	1	0	1	0	1	1	0	1	0	0
442	1	0	0	1	0	1	1	0	1	0	0
445	0	0	0	1	0	1	1	0	1	0	0
447	0	1	0	1	0	1	1	0	1	0	0
450	1	1	0	1	0	1	1	0	1	0	0
452	1	0	0	1	0	1	1	0	1	0	0
455	0	0	0	1	0	1	1	0	1	0	0
457	0	1	0	0	0	1	1	0	1	0	0
460	1	1	0	0	0	1	1	0	1	0	0
462	1	0	0	0	0	1	1	0	1	0	0
465	0	0	0	0	0	1	1	0	1	0	0
467	0	1	0	1	0	1	1	0	1	0	0
470	1	1	0	1	0	1	1	0	1	0	0
472	1	0	0	1	0	1	1	0	1	0	0
475	0	0	0	1	0	1	1	0	1	0	0
477	0	1	0	1	0	1	1	0	1	0	0
480	1	1	0	1	0	1	1	0	1	0	0
482	1	0	0	1	0	1	1	0	1	0	0
485	0	0	0	1	0	1	1	0	1	0	0
486	0	0	0	1	0	1	1	0	0	0	0
487	0	1	0	1	0	1	1	0	0	0	0
489	0	1	0	1	0	1	1	0	0	1	1
490	1	1	0	1	0	1	1	1	0	1	1
491	1	1	0	1	0	1	1	0	0	1	1
492	1	0	0	1	0	1	1	0	0	1	1
494	1	0	0	1	0	1	1	0	1	1	1
495	0	0	0	1	0	1	1	0	1	1	1
497	0	1	0	1	0	1	1	0	1	1	1
500	1	1	0	1	0	1	1	1	1	1	1
501	1	1	0	1	0	1	1	0	1	1	1
502	1	0	0	1	0	1	1	0	1	1	1
505	0	0	0	1	0	1	1	0	1	1	1
507	0	1	0	0	0	1	1	0	1	1	1
510	1	1	0	0	0	1	1	1	1	1	1
511	1	1	0	0	0	1	1	0	1	1	1
512	1	0	0	0	0	1	1	0	1	1	1
515	0	0	0	0	0	1	1	0	1	1	1
517	0	1	0	0	0	1	1	0	1	1	1
520	1	1	0	0	0	1	1	1	1	1	1

TIME	(CLOCK)	75	(RESET)	(SRLIN)	184	185	192	183	70	(015)	(014)
521	1	1	0	0	0	1	1	0	1	1	1
522	1	0	0	0	0	1	1	0	1	1	1
525	0	0	0	0	0	1	1	0	1	1	1
527	0	1	0	0	0	1	1	0	1	1	1
530	1	1	0	0	0	1	1	0	1	1	1
532	1	0	0	0	0	1	1	0	1	1	1
535	0	0	0	0	0	1	1	0	1	1	1
537	0	1	0	0	0	1	1	0	1	1	1
540	1	1	0	0	0	1	1	0	1	1	1
542	1	0	0	0	0	1	1	0	1	1	1
545	0	0	0	0	0	1	1	0	1	1	1
547	0	1	0	0	0	1	1	0	1	1	1
550	1	1	0	0	0	1	1	0	1	1	1
552	1	0	0	0	0	1	1	0	1	1	1
555	0	0	0	0	0	1	1	0	1	1	1
557	0	1	0	0	0	1	1	0	1	1	1
560	1	1	0	0	0	1	1	0	1	1	1
562	1	0	0	0	0	1	1	0	1	1	1
565	0	0	0	0	0	1	1	0	1	1	1
567	0	1	0	0	0	1	1	0	1	1	1
570	1	1	0	0	0	1	1	0	1	1	1
572	1	0	0	0	0	1	1	0	1	1	1
575	0	0	0	0	0	1	1	0	1	1	1
577	0	1	0	0	0	1	1	0	1	1	1
580	1	1	0	0	0	1	1	0	1	1	1
582	1	0	0	0	0	1	1	0	1	1	1
585	0	0	0	0	0	1	1	0	1	1	1
587	0	1	0	0	0	1	1	0	1	1	1
590	1	1	0	0	0	1	1	0	1	1	1
592	1	0	0	0	0	1	1	0	1	1	1
595	0	0	0	0	0	1	1	0	1	1	1
597	0	1	0	0	0	1	1	0	1	1	1
600	1	1	0	0	0	1	1	0	1	1	1
602	1	0	0	0	0	1	1	0	1	1	1
605	0	0	0	0	0	1	1	0	1	1	1
607	0	1	0	0	0	1	1	0	1	1	1
610	1	1	0	0	0	1	1	0	1	1	1
612	1	0	0	0	0	1	1	0	1	1	1
615	0	0	0	0	0	1	1	0	1	1	1
617	0	1	0	0	0	1	1	0	1	1	1
620	1	1	0	0	0	1	1	0	1	1	1
622	1	0	0	0	0	1	1	0	1	1	1
625	0	0	0	0	0	1	1	0	1	1	1

TIME	(CLOCK)	75	(RESET)	(SRLIN)	184	185	192	183	70	(015)	(014)
627	0	1	0	0	0	1	1	0	1	1	1
630	1	1	0	0	0	1	1	0	1	1	1
632	1	0	0	0	0	1	1	0	1	1	1
635	0	0	0	0	0	1	1	0	1	1	1
637	0	1	0	0	0	1	1	0	1	1	1
640	1	1	0	0	0	1	1	0	1	1	1
642	1	0	0	0	0	1	1	0	1	1	1
645	0	0	0	0	0	1	1	0	1	1	1
646	0	0	0	0	0	1	1	0	0	1	1
647	0	1	0	0	0	1	1	0	0	1	1
648	0	1	0	0	0	1	1	0	0	0	0
650	1	1	0	0	0	1	1	0	0	0	0
652	1	0	0	0	0	1	1	0	0	0	0
654	1	0	0	0	0	1	1	0	1	0	0
655	0	0	0	0	0	1	1	0	1	0	0
657	0	1	0	0	0	1	1	0	1	0	0
660	1	1	0	0	0	1	1	0	1	0	0

1 PAGE 2. 1

```
                (    (    (    (    (    (    (    (    (    (    (
                0    0    0    0    0    0    0    0    0    0    0
                1    1    1    1    9    8    7    6    5    4    3
                3    2    1    0    )    )    )    )    )    )    )
                )    )    )    )

        TIME
          0   XXX  XXX  XXX  XXX  XXX  XXX  XXX  XXX  XXX  XXX  XXX
        169     1    1    1    1    1    1    1    1    1    1    1
        328   0    0    0    0    0    0    0    0    0    0    0
        489   0      1    1  0      1    1    1    1  0      1    1
        648   0    0    0    0    0    0    0    0    0    0    0
```

1 PAGE 3. 1

```
                (    (    (
                0    0    0
                2    1    0
                )    )    )

        TIME
          0   XXX  XXX  XXX
        169     1    1    1
        328   0    0    0
        489   0      1    1
```

1

TCC 31. END $

*** 430 SIGNAL VALUE RECORDS ARE WRITTEN TO THE SAVE FILE. **

END

DTIC

5-86